User's Manual

EBC-3410

All-in-One NS Geode GX1
Single Board with LCD, AC97 Audio,
& Dual 10/100 Base-Tx Ethernet

1st Ed. - 28 July 2001

FCC STATEMENT

THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE

RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINTST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

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Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 EBC-3410 All-in-One NS Geode GX1 Computing Module
- 1 Quick Installation Guide
- 1 Audio jacks and USB connector daughter board
- 1 CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities
  - Latest BIOS (as of the CD-ROM was made)
- Cable set includes the followings:
  - 1 PS/2 keyboard and mouse Y cable (6-pin, Mini-DIN)
  - 1 IDE HDD cable (44-pin, pitch 2.0mm)
  - 1 FDD cable (34-pin, pitch 2.0mm)
  - 1 bracket with one Printer port cable (26-pin, pitch 2.0mm) and one Serial port cable (10-pin, pitch 2.0mm)
  - 2 flat cables (10-pin, pitch 2.0mm) for connecting the Audio/USB daughter board to the EBC-3410

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

Document Amendment History

Revision	Date	By	Comment
1st	Jul. 01.	Philip Chang	Initial Release

1. Manual Objectives

This manual describes in detail the BCM EBC-3410 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with EBC-3410 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

2. Introduction

2.1 System Overview

The EBC-3410 is an ultra compact 3.5" FDD-size Single Board Computer that equips with low-power NS Geode GX1 processor, LCD interface, AC97 Audio and dual PCI-bus Ethernet interfaces.

Targeting on the rapid growing networking and embedded system markets, the EBC-3410 is the first 3.5" SBC designed with dual high-end PCI-bus Realtek RTL8139C 10/100Base-Tx Ethernet controllers. Making it the perfect solution for popular networking devices like Gateway, Router, Thin Server, Firewall and E-Box.

Running on the NS Geode GX1 200/300*MHz Low Power CPU and CS5530A multimedia companion chipset, the EBC-3410 is also ideal for the demanding Internet Access Devices or Mobile Applications that require a low-power and low-heat dissipation Single Board Computer, such as WBT (Windows Based Terminal), Thin Client, STB (Set Top Box), Web Phone, and other Information Appliances.

Other impressive features include a built-in 40-pin TFT LCD interface, the AC97 Audio, a Compact Flash socket for type I/ II Compact Flash storage card, two serial ports, one parallel port, and a 144-pin SODIMM socket allowing for up to 256MB of SDRAM to be installed.

* Special request for 300MHz Processor.

2.2 System Specifications

General Functions

CPU: Onboard NS Geode GX1 200MHz (available in different speeds by special order), BGA package

BIOS: Award 256KB Flash BIOS

Chipset: NS Geode CS5530A

I/O Chipset: Winbond W83977F-A

Memory: Onboard one 144-pin SODIMM socket supports up to 256 Mbytes SDRAM

Enhanced IDE: Supports two IDE devices. Supports Ultra DMA/33 mode with data transfer rate up to 33MB/sec.

FDD interface: Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB, and 2.88MB)

Parallel port: Internal header for bi-directional parallel port x 1. Supports SPP, ECP, and EPP modes

Serial port: One external DB-9 connector supports RS-232 x 1, one internal header supports RS-232/422/485 x 1. Ports can be configured as COM1, COM2, COM3, COM4, or disabled individually. (16C550 equivalent)

IR interface: Supports one IrDA Tx/Rx header

KB/Mouse connector: External mini-DIN PS2 Keyboard/Mouse connector x 1

USB connectors: One 5 x 2 header onboard supports dual USB ports

Watchdog Timer: Can generate a system reset, IRQ15 or NMI. Software selectable time-out interval (16 sec. ~ 127min., 30 sec./step)

DMA: 7 DMA channels (8237 equivalent)

Interrupt: 15 interrupt levels (8259 equivalent)

Power management: I/O peripheral devices support power saving and

doze/standby/suspend modes. APM 1.2 compliant.

Flat Panel/CRT Interface

Chipset: NS Geode CS5530A

Display memory: Shared display memory up to 4MB

Display type: Supports non-interlaced CRT and up to 18-bit TFT LCD displays. Can display both CRT and flat panel simultaneously

Resolution: Up to 1280x1024x8 bpp and 1024x768x16 bpp

Audio Interface

Chipset: NS Geode CS5530A

Audio controller: AC97 ver.2.0 compliant interface, Multi-stream Direct Sound and Direct Sound 3D acceleration

Audio interface: Microphone in, Line in, CD audio in, line out, Speaker L, Speaker R

Ethernet Interface

Chipset: Dual Realtek RTL8139C PCI-bus Ethernet controllers onboard

Ethernet interface: PCI 100/10 Mbps, IEEE 802.3U compatible

Remote Boot-ROM: For diskless system

SSD Interface

One CF socket supports Type I / II Compact Flash Card

Expansion Interface

One 16-bit 104-pin connector onboard

Connectors

External connectors: VGA (DB-15), COM 1 (DB-9), Ethernet (RJ-45) x 2, KB/Mouse (Mini-DIN)

Power connectors: 4-pin HDD type

Mechanical and Environmental

Power supply voltage: +5V (4.75V to 5.25V)

Typical power requirement: 5V @ 2A w/ GX1 300MHz

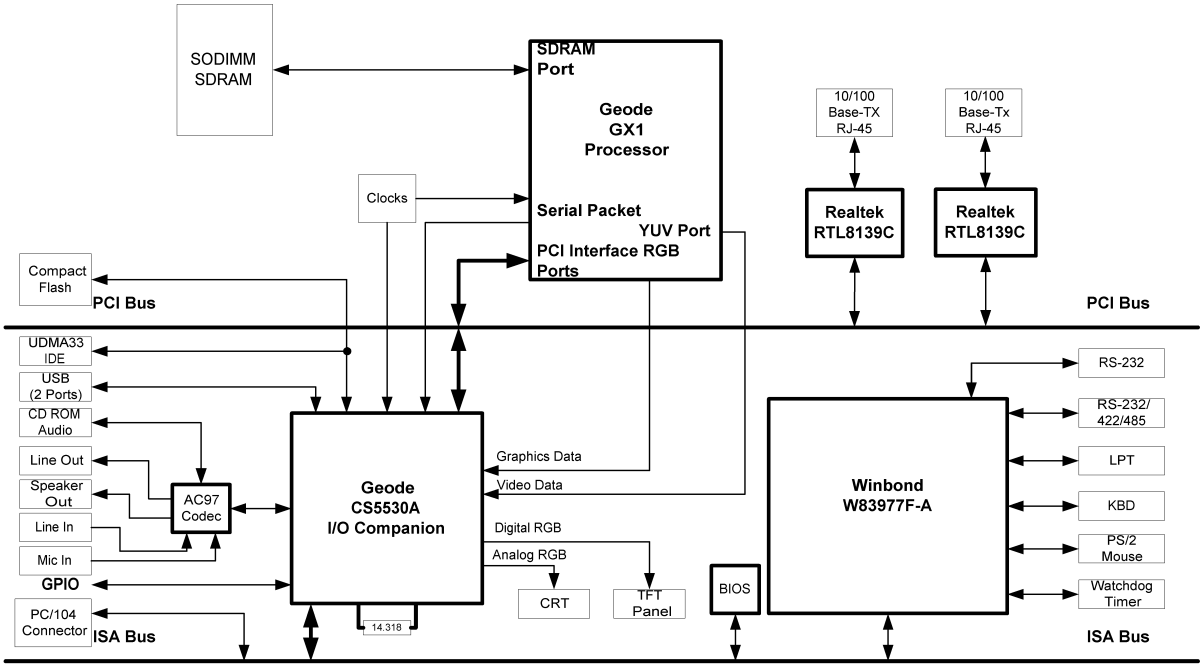
Operating temperature: 32 to 140°F (0 to 60°C)

Board size: 146mm x 101mm (3.5” FDD-size)

Weight: 0.4 Kg

2.3 Architecture Overview

The following block diagram shows the architecture and main components of EBC-3410.



The two key components on board are the NS Geode GX1 CPU and the CS5530A companion chip. These two devices provide the ISA and PCI bus to which all the major components are attached.

The following sections provide detail information about the functions provided onboard.

2.3.1 CPU/GX1 and CS5530A

The NS Geode GX1 along with the CS5530A companion chip provide the basic functionality and buses of the system:

- Interface to SDRAM, 64-bit data bus. PC100 compliant SDRAM must be used.
- PCI interface provided by GX1 CPU.
- PCI to ISA Bridge provided by CS5530A.
- VGA controller with video memory shared with system memory (UMA). The image data is transferred to the companion chip by means of *Pixel* bus.
- CRT and TFT interface. Data provided by the *Pixel* and *Video* interface from the CPU. The TFT interface and SA part of the ISA bus share pins as described later.
- Video interface from GX1 to the CS5530A. This data-stream is buffered and multiplexed with the *Pixel* bus for windowed video viewing. This interface may assist the processor in connection motion picture decoding.
- USB integrated in the CS5530A.
- IDE interface support Ultra DMA. Two connectors are provided: A 44 pin pitch 2.0mm standard IDE interface on the primary controller and a Compact Flash connector on the secondary controller.
- Digital audio interface to an AC97 compliant audio Codec.

2.3.2 XPRESS Graphics

The XPRESS Graphics is based on the GX1 CPU and the CS5530A Companion chip and this graphics controller is very cost efficient since almost no additional components are required. This is achieved by using the SDRAM as frame-buffer and by integrating the graphics engine and display interface in the GX1 CPU and the CS5530A companion chip. This controller provides a CRT as well as a TFT interface which support the modes listed below:

The TFT panel interface is available as a parallel interface in the CN6 connector.

2.3.3 PCI Bus

The PCI-bus on the board is provided by the GX1 CPU and will always run at 33MHz.

The GX1 CPU provides support for up to three bus masters. These bus master signals are used by the CS5530A and dual Realtek RTL8139C Ethernet controllers.

2.3.4 PC/104 Interface

The CS5530A companion chip provides a PCI-ISA Bridge that may operate in master or slave mode. EBC-3410 only support ISA slave mode. ISA master mode allows an ISA board to grant the bus and thereby get the bus master status. The bus master has the ability to generate bus cycles and thereby transfer data without involvement of the CPU or DMA (Direct memory access). However, ISA add-on card, which utilizes the bus master mode, is very rare today. A 104-pin PC/104 connector is equipped onboard for future expansion.

2.3.5 SDRAM Interface

This board uses SDRAM in the compact SODIMM-144 form factor. 3.3V PC 100 SDRAM modules are recommended to be use.

2.3.6 TFT Panel Interface

An alternative display to the standard CRT monitor is a digital flat panel interface in which the colour of each pixel is digitally encoded. The panel data may be transferred in parallel where the colour of each pixel is transferred over a number of signal lines at rates up to 65MHz.

The parallel interface is only suitable for short distance (less than 50 cm) and is typically implemented by using of ribbon cables. One should be careful in the EMC design of the box and cabling when this interface is used.

It should also be noted that the signal level of this interface is 3.3V, but does comply with the TTL signal levels. Some - most older displays require 5V signal level.

2.3.7 Audio

The CS5530A companion chip provides audio support through an AC97 Codec interface. The audio Codec provides mixing of the analog signals as well as Digital/Analog conversion. The following analog interfaces are provided.

- Line-in, stereo.
- CD-ROM input, stereo.
- Microphone, single input with microphone bias circuit.
- Line-out, stereo.

Access to the audio signals is provided by a 5 x 2 header (CN10) or by an optional audio bracket.

2.3.8 IDE Interface

A primary as well as a secondary IDE controller is provided by the CS5530A companion chip which supports Ultra DMA mode and PCI bus mastering for the data transfer.

A standard IDC 44-pin connector and a Compact Flash type II connector on the backside of this board provide access to these controllers.

2.3.9 USB

The USB interface provides two USB channels that are controlled by the CS5530A.

A 5x2 header provide USB signals to connect to an USB adapter board are available. (Optional)

2.3.10 Realtek RTL8139C Ethernet Controller

The Realtek RTL8139C is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that is capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management.

2.3.11 Winbond W83977F-A

The Winbond W83977F-A Super I/O chip provides most input / output interfaces of the system as the following:

- COM 1. Operates in RS-232 mode through a charge pump driver. Only 5V supply is required
- COM 2. A RS-232/RS-422/RS-485 driver is used whereby RS-232, RS-422 and RS-485 are provided. Modes are select by hardware jumper. Driver uses charge pumps whereby only +5V is required
- LPT. Support for SPP, EPP and ECP modes
- Floppy interface
- Keyboard interface
- PS/2 Mouse interface
- IrDA interface for infrared communication. This interface shares the controller of COM2
- Provision of buffered ISA data bus for BIOS (denoted *XDBus)*
- NVRAM with battery backup for BIOS configuration and real time clock
- Watchdog timer

2.3.12 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

3. Hardware Configuration

3.1 Installation Procedure

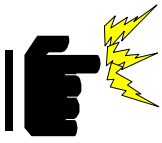
1. Turn off the power supply.
2. Insert the SODIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1.
5. Turn on the power.
6. Enter the BIOS SETUP by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilised, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

3.2 Safety Precautions

3.2.1 Warning!

Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

3.2.2 Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Installing DRAM (SODIMMs)

3.3.1 System Memory

The reverse side of the EBC-3410 contains a socket for 144-pin dual inline memory module (SODIMM). The socket uses 3.3 V unbuffered synchronous DRAM (SDRAM). SODIMM module is available in capacities of 32, 64, 128, or 256 MB. The socket can be filled in the SODIMM of any size, giving your EBC-3410 single board between 32 and 256 MB of memory.

3.3.2 Supplementary Information About SODIMM

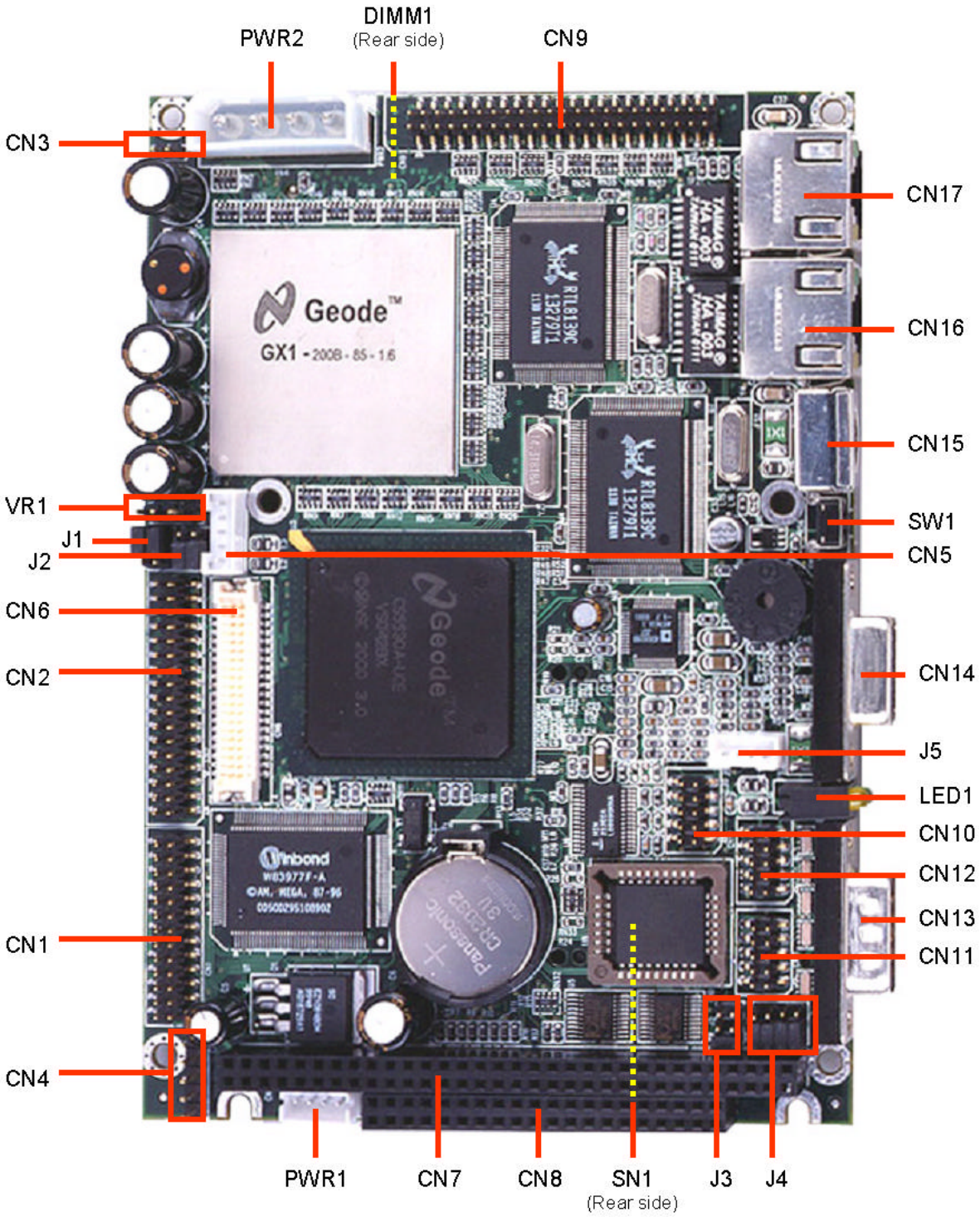
Your EBC-3410 accepts both regular and PC-100 SDRAM SODIMM Module (with or without parity). Single-sided modules are typically 64 MB; double-sided modules are usually 32 or 128 MB.

3.3.3 Memory Installation Procedures

Press the SODIMM module right down into the socket, until you hear a click. This is when the two handles have automatically locked the memory module into the correct position of the SODIMM socket. (See Figure below) To take away the memory module, just push both handles outward, and the memory module will be ejected by the mechanism in the socket.

3.4 Jumper & Connector

3.4.1 Jumper & Connector Layout



3.4.2 Jumper & Connector List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

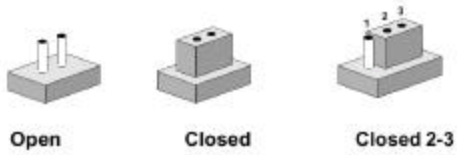
Jumpers		
Label	**Function**	**Note**
J1	LCD driving & backlight voltage select	3 x 2 header, pitch 2.0mm
J2	Clear CMOS / LCD clock signal select	3 x 2 header, pitch 2.0mm
J3, J4	COM2 RS-232/422/485 select	3 x 2 header, pitch 2.0mm 4 x 3 header, pitch 2.0mm (J4)

Connectors		
Label	**Function**	**Note**
CN1	Parallel port connector	13 x 2 header, pitch 2.0mm
CN2	Floppy connector	17 x 2 header, pitch 2.0mm
CN3	System fan connector	2 x 1 header, pitch 2.0mm
CN4	IrDA connector	5 x 1 header, pitch 2.54mm
CN5	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
CN6	TFT panel connector	HIROSE DF13-40DP-1.25V
CN7, CN8	PC/104 connector	
CN9	IDE connector	22 x 2 header, pitch 2.0mm
CN10	Audio connector	5 x 2 header, pitch 2.0mm
CN11	Serial port 2 connector	5 x 2 header, pitch 2.0mm
CN12	USB connector	5 x 2 header, pitch 2.0mm
CN13	Serial port 1 connector	DB-9 male connector
CN14	CRT connector	DB-15 female connector
CN15	Keyboard and PS/2 mouse connector	6-pin mini DIN
CN16	10/100Base-Tx Ethernet 1 connector	RJ-45
CN17	10/100Base-Tx Ethernet 2 connector	RJ-45 (EBC-3410 only)
J5	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
PWR1	Auxiliary power connector	4 x 1 wafer, pitch 2.0mm
PWR2	Power connector	Molex A-8981-04V5
SN1	Compact Flash connector	
SW1	Reset button	
LED1	Power & HDD indicator	
VR1	LCD backlight brightness adjustment connector	
DIMM1	144-pin SODIMM socket	

3.5 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



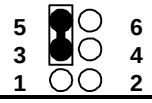
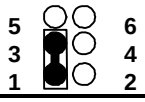
The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

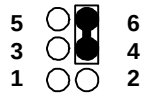
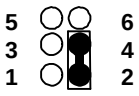
If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

3.5.1 LCD Driving & Backlight Voltage Select (J1)

You can select the TFT connector CN6 driving (pin 5 and pin 6) and backlight (pin 1 and pin 2) voltage by setting J1. The configurations are as follows.

LCD Driving Voltage Select (J1 / Pin 1,3,5)		
	+3.3V*	+5V
J1		

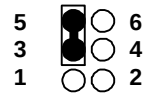
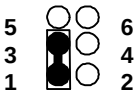
* default

LCD Backlight Voltage Select (J1 / Pin 2,4,6)		
	+12V*	+5V
J1		

* default

3.5.2 Clear CMOS (J2 / Pin 1, 3, 5)

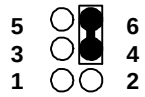
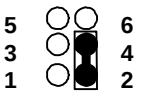
You can use J2 to clear the CMOS data if necessary. To reset the CMOS data, set J2 to 3-5 closed for just a few seconds, and then move the jumper back to 1-3 closed.

Clear CMOS (J2 / Pin 1, 3, 5)		
	Clear CMOS	Protect*
J2		

* default

3.5.3 LCD Clock Signal Select (J2 / Pin 2, 4, 6)

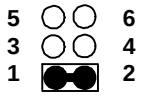
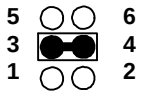
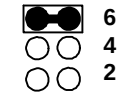
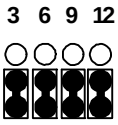
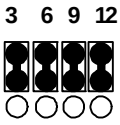
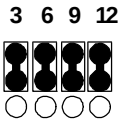
You can select the LCD control signal by setting J2. The following charts show the available option.

LCD Clock Signal Select (J2 / Pin 2, 4, 6)		
	-SHFCLK	SHFCLK*
J2		

* default

3.5.4 COM2 RS-232/422/485 Select (J3, J4)

The EBC-3410 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting J3 & J4.

COM2 RS-232/422/485 Select (J3, J4)			
	RS-232*	RS-422	RS-485
J3			
J4			

* default

3.6 Connector Definitions

3.6.1 Parallel Port Connector (CN1)

Signal	PIN		Signal
STB#	1	2	AFD#
PD0	3	4	ERR#
PD1	5	6	INIT#
PD2	7	8	SLIN#
PD3	9	10	GND
PD4	11	12	GND
PD5	13	14	GND
PD6	15	16	GND
PD7	17	18	GND
ACK#	19	20	GND
BUSY	21	22	GND
PE	23	24	GND
SLCT	25	26	GND

3.6.2 DB25 Parallel Port Connector

Signal	PIN		Signal
STB#	1		
		14	AFD#
PD0	2		
		15	ERR#
PD1	3		
		16	INIT#
PD2	4		
		17	SLIN#
PD3	5		
		18	GND
PD4	6		
		19	GND
PD5	7		
		20	GND
PD6	8		
		21	GND
PD7	9		
		22	GND
ACK#	10		
		23	GND
BUSY	11		
		24	GND
PE	12		
		25	GND
SLCT	13		

3.6.3 Signal Description – Parallel Port Connector (CN1)

The following signal description covers the signal definitions, when the parallel port is operated in standard centronic mode. The parallel port controller also supports the fast EPP and ECP modes.

PD [7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

3.6.4 Floppy Connector (CN2)

Signal	PIN		Signal
DSKCHG#	34	33	GND
SIDE1#	32	31	GND
RDATA#	30	29	GND
WPT#	28	27	GND
TRAK0#	26	25	GND
WE#	24	23	GND
WD#	22	21	GND
STEP#	20	19	GND
DIR#	18	17	GND
MOB#	16	15	GND
DSA#	14	13	GND
DSB#	12	11	GND
MOA#	10	9	GND
INDEX#	8	7	GND
DRVDEN1#	6	5	GND
NC	4	3	GND
DRVDEN0#	2	1	GND

3.6.5 Signal Description – Floppy Connector (CN2)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRVDEN0/1#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

3.6.6 System Fan Connector (CN3)

Signal	PIN
VCC	1
GND	2

3.6.7 IrDA Connector (CN4)

Signal	PIN
VCC	1
NC	2
IRRX	3
GND	4
IRTX	5

3.6.8 Signal Configuration – IrDA Connector (CN4)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

3.6.9 LCD Inverter Connector (CN5)

Signal	PIN
+12V	1
GND	2
ENBKL	3
VR	4
VCC	5

Note:

For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal (pin 4) controlled by VR1. Please see the VR1 section for detailed circuitry information.

3.6.10 Signal Configuration – LCD Inverter Connector (CN5)

VR	Vadj = 5V ~ 0V.
ENBKL	LCD backlight ON/OFF control signal.

3.6.11 TFT Panel Connector (CN6)

Signal	PIN		Signal
ENBKL	39	40	ENVEE
M	37	38	LP
SHFCLK	35	36	FLM
GND	33	34	GND
P22	31	32	P23
P20	29	30	P21
P18	27	28	P19
NC	25	26	NC
P14	23	24	P15
P12	21	22	P13
P10	19	20	P11
NC	17	18	NC
P6	15	16	P7
P4	13	14	P5
P2	11	12	P3
NC	9	10	NC
NC	7	8	GND
VDDSAFE3	5	6	VDDSAFE3
GND	3	4	GND
VDDSAFE5	1	2	VDDSAFE5

3.6.12 Signal Description – TFT Panel Connector (CN6)

P [23:18] P [15:10] P [7:2]	Flat panel data output for 9, 12, or 18 bit TFT flat panels. Refer to table below for configurations for various panel types. The flat panel data and control outputs are all on-board controlled for secure power-on/off sequencing
SHFCLK	Shift Clock. Pixel clock for flat panel data
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronization)
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronization)
M	Multipurpose signal, function depends on panel type. May be used as AC drive control signal or as BLANK# or Display Enable signal
ENBKL	Enable backlight signal. This signal is controlled as a part of the panel power sequencing
ENVEE	Enable VEE. Signal to control the panel power-on/off sequencing. A high level may turn on the VEE (LCD bias voltage) supply to the panel
VDDSAFE5	LCD Backlight Voltage +5V or +12V* selected by J1 / Pin 2, 4, 6
VDDSAFE3	LCD Driving Voltage +5V or 3.3V* selected by J1 / Pin 1, 3, 5

* default

3.6.13 Signal Configuration – TFT Panel Displays

Pin name	18 Bit TFT	12 Bit TFT	9 Bit TFT/ 640 x 480	9 Bit TFT/ 1024 x 768
P23	R5	R5	R5	R5 (Even)
P22	R4	R4	R4	R4 (Even)
P21	R3	R3	R3	R3 (Even)
P20	R2	R2	-	R5 (Odd)
P19	R1	-	-	R4 (Odd)
P18	R0	-	-	R3 (Odd)
P15	G5	G5	G5	G5 (Even)
P14	G4	G4	G4	G4 (Even)
P13	G3	G3	G3	G3 (Even)
P12	G2	G2	-	G5 (Odd)
P11	G1	-	-	G4 (Odd)
P10	G0	-	-	G3 (Odd)
P7	B5	B5	B5	B5 (Even)
P6	B4	B4	B4	B4 (Even)
P5	B3	B3	B3	B3 (Even)
P4	B2	B2	-	B5 (Odd)
P3	B1	-	-	B4 (Odd)
P2	B0	-	-	B3 (Odd)

Note:

The principle of attachment of TFT panels is that the bits for red, green, and blue use the most significant bits and skip the least significant bits if the display interface width of the TFT panel is insufficient.

3.6.14 PC/104 Connector (CN7, CN8)

Signal	PIN		PIN		Signal
GND	B32	A32			GND
GND	B31	A31			SA0
OSC	B30	A30			SA1
VCC	B29	A29			SA2
BALE	B28	A28			SA3
NC			C19	D19	GND
TC	B27	A27			SA4
SD15			C18	D18	GND
DACK2#	B26	A26			SA5
SD14			C17	D17	MASTER#
IRQ3	B25	A25			SA6
SD13			C16	D16	VCC
IRQ4	B24	A24			SA7
SD12			C15	D15	DRQ7
IRQ5	B23	A23			SA8
SD11			C14	D14	DACK7#
IRQ6	B22	A22			SA9
SD10			C13	D13	DRQ6
IRQ7	B21	A21			SA10
SD9			C12	D12	DACK6#
SYSCLK	B20	A20			SA11
SD8			C11	D11	DRQ5
REFRESH#	B19	A19			SA12
SMEMW#			C10	D10	DACK5#
DRQ1	B18	A18			SA13
SMEMR#			C9	D9	DRQ0
DACK1#	B17	A17			SA14
LA17			C8	D8	DACK0#
DRQ3	B16	A16			SA15
LA18			C7	D7	IRQ14
DACK3#	B15	A15			SA16
LA19			C6	D6	IRQ15
IOR#	B14	A14			SA17
LA20			C5	D5	IRQ12
IOW#	B13	A13			SA18
LA21			C4	D4	IRQ11
SMEMR#	B12	A12			SA19
LA22			C3	D3	IRQ10
SMEMW#	B11	A11			AEN
LA23			C2	D2	IOCS16#
GND	B10	A10			IOCHRDY
SBHE#			C1	D1	MEMCS16#
+ 12 V	B9	A9			SD0
GND			C0	D0	GND
OWS#	B8	A8			SD1
- 12 V	B7	A7			SD2
DRQ2	B6	A6			SD3
- 5 V	B5	A5			SD4
IRQ9	B4	A4			SD5
VCC	B3	A3			SD6
RESETDRV	B2	A2			SD7
GND	B1	A1			IOCHCHK#

3.6.15 Signal Description – PC/104 Connector (CN7, CN8)

3.6.15.1 Address

LA [23:17]	The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA [19:0]	System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit
SBHE#	This signal is an active low signal, that indicates that a byte is being transferred on the upper byte (SD [15:8]) of the 16 bit bus. All bus masters will drive this line with a tri-state driver.

3.6.15.2 Data

SD [15:8]	These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.
SD [7:0]	These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus:

SBHE#	SA0	SD15-SD8	SD7-SD0	Action
0	0	ODD	EVEN	Word transfer
0	1	ODD	ODD	Byte transfer on SD15-SD8
1	0	-	EVEN	Byte transfer on SD7-SD0
1	1	-	ODD	Byte transfer on SD7-SD0

`

3.6.15.3 Commands

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. BALE is driven by the permanent master with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O writes operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

3.6.15.4 Transfer Response

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only.
0WS#	This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a non-maskable interrupt.

3.6.15.5 Controls

SYSCLK	This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the setup made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PC-AT/PC104 bus timing is based on this clock signal.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The signal is driven by the permanent master.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

3.6.15.6 Interrupts

IRQ [3:7], IRQ [9:12], IRQ [14:15]	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked.

3.6.15.7 Bus Arbitration

DRQ [0:3], DRQ [5:7]	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus.
DACK [0:3]#, DACK [5:7]#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. They are continuously driven by a totem pole driver for DMA channels attached.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the address lines are driven by the DMA controller. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active $DACK_n$# should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver.
TC	This active high signal is asserted during a read or write command indicating that the DMA controller has reached a terminal count for the current transfer. $DACK_n$# must be presented by the bus adapter to validate the TC signal.
MASTER#	This signal is not supported by the chipset.

3.6.16 IDE Connector (CN9)

Signal	PIN		Signal
RESET#	1	2	GND
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
GND	19	20	NC
DREQ	21	22	GND
IOW#	23	24	GND
IOR#	25	26	GND
IORDY	27	28	GND
DACK#	29	30	GND
IRQ14	31	32	NC
DA1	33	34	NC
DA0	35	36	DA2
DCS1#	37	38	DCS3#
DACT#	39	40	GND
VCC	41	42	VCC
GND	43	44	NC

3.6.17 Signal Description – IDE Connector (CN9)

The IDE interface supports PIO modes 0 to 4 and Bus Master IDE. Data transfer rates up to 33 MB/Sec is possible.

DA [2:0]	IDE Address Bits. These address bits are used to access a register or data port in a device on the IDE bus.
DCS1#, DCS3#	IDE Chip Selects. The chip select signals are used to select the command block registers in an IDE device. DCS1# selects the primary hard disk.
D [15:0]	IDE Data Lines. D [15:0] transfers data to/from the IDE devices.
IOR#	IDE I/O Read. Signal is asserted on read accesses to the corresponding IDE port addresses.
IOW#	IDE I/O Write. Each signal is asserted on write accesses to corresponding the IDE port addresses.
IORDY	When deasserted, these signals extend the transfer cycle of any host register access when the device is not ready to respond to the data transfer request.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
DREQ	The DREQ is used to request a DMA transfer from the CS5530A. The direction of the transfers is determined by the IOR#/IOW# signals.
DACK#	DMA Acknowledge. The DACK# acknowledges the DREQ request to initiate DMA transfers.
DACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the hard disk type, normally active low. The signal is routed directly to the LED1.

3.6.18 Audio Connector (CN10)

Signal	PIN		Signal
NC	10	9	NC
Mic Bias	8	7	Mic
Line-In L	6	5	Line-In R
GND	4	3	GND
Line-Out L	2	1	Line-Out R

3.6.19 Signal Description – Audio Connector (CN10)

SPK L/R	Left and right speaker output. These are the speaker outputs directly from the speaker amplifier. Coupling capacitors must be used in order to avoid DC-currents in the speakers. If the Audio Bracket is used these signals are supplied on the PCB. GND should be used as return for each speaker. Maximum power: 0.5W@4 Ω load for each channel.
Mic / Mic Bias	The MIC signal is used for microphone input. This input is fed to the left microphone channel. Mic Bias provides 3.3V supplied through 3.2K Ω with capacitive decoupling to GND. This signal may be used for bias of some microphone types.
Line-In L/R	Left and right line in signals.
Line-Out L/R	Left and right line out signals. Both signals are capacitor coupled and should have GND as return.

3.6.20 Pin Header Serial Port 2 Connector in RS-232 Mode (CN11)

Signal	PIN		Signal
NC	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
DTR	4	3	TxD
RxD	2	1	DCD

3.6.21 Serial Port 2 with External DB9 Connector

Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.6.22 Signal Description – Serial Port 2 – COM2 in RS-232 Mode (CN11)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.6.23 Pin Header Serial Port 2 Connector in RS-422 Mode (CN11)

Signal	PIN		Signal
NC	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
TxD+	4	3	TxD-
RxD-	2	1	RxD+

3.6.24 Signal Description – Serial Port 2 – COM2 in RS-422 Mode (CN11)

TxD +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the TxD line driver is enabled through the Serial Port 2's DTR signal. (Modem control register)
RxD +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.
RTS +/-	Request To Send. The level of this differential signal pair output is controlled through the Serial Port 2's RTS signal (Modem control register).
CTS +/-	Clear To Send. The level of this differential signal pair input could be read from the Serial Port 2's CTS signal. (Modem control register)

3.6.25 Pin Header Serial Port 2 Connector in RS-485 Mode (CN11)

Signal	PIN		Signal
NC	10	9	CTS/RTS+
NC	8	7	CTS/RTS-
NC	6	5	GND
RxD/TxD+	4	3	RxD/TxD-
NC	2	1	NC

3.6.26 Signal Description – Serial Port 2 – COM2 in RS-485 Mode (CN11)

RxD/TxD +/-	Bi-directional data signal pair. Received data is available in Serial Port 2 Receiver Buffer Register. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication line, if the TxD line driver is enabled through the Serial Port 2's DTR signal (Modem control register). The data transmitted will simultaneously be received the in Serial Port 2 Receiver Buffer Register.
CTS/RTS +/-	Bi-directional control signal pair. The level of this differential signal pair could be read from the Serial Port 1's CTS signal (Modem control register). The level of this differential signal pair could be controlled through the Serial Port 2's RTS signal (Modem control register).

Warning: Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperatures reach 150 °C.

RS-422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typ. 100-120 Ω). The resistors could be placed in the connector housing.

RS-485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 Ω). Stubs to substations should be avoided.

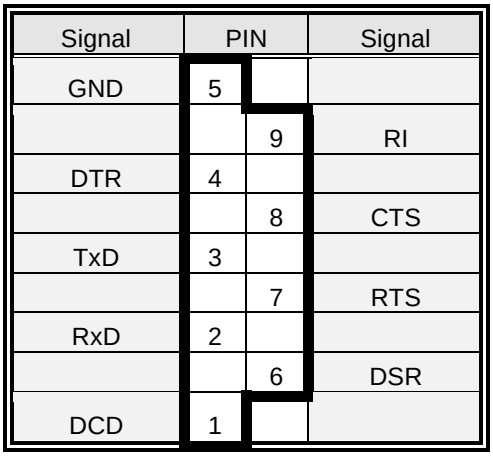
3.6.27 USB Connector (CN12)

Signal	PIN CH1	PIN CH2	Signal
VCC2	10	9	GND
D2-	8	7	GND
D2+	6	5	D1+
GND	4	3	D1-
GND	2	1	VCC1

3.6.28 Signal Description – USB Connector (CN12)

D1+ / D1-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D2+ / D2-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

3.6.29 DB9 Serial Port 1 Connector in RS-232 Mode (CN13)

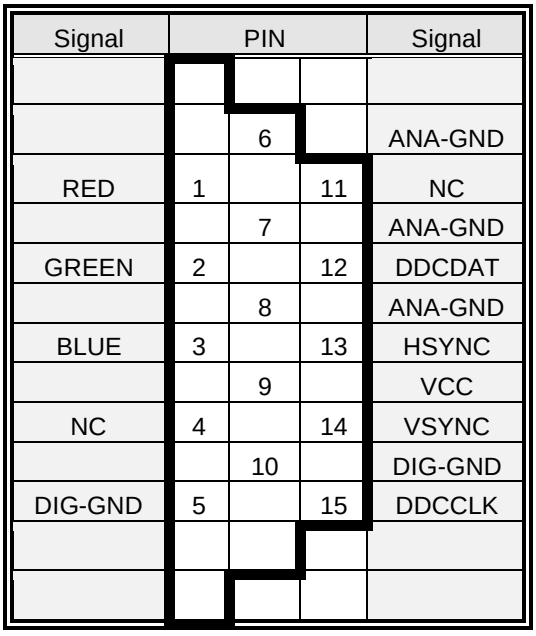


Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

3.6.30 Signal Description – Serial Port 1 – COM1 in RS-232 Mode (CN13)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.

3.6.31 CRT Connector (CN14)

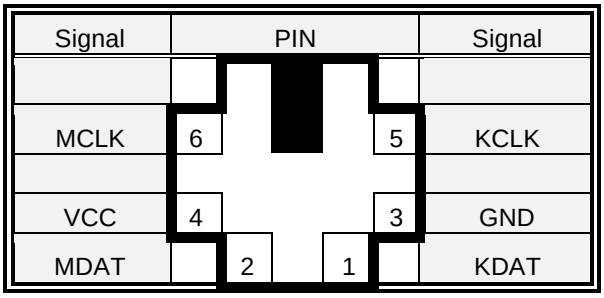


Signal	PIN			Signal
		6		ANA-GND
RED	1		11	NC
		7		ANA-GND
GREEN	2		12	DDCDAT
		8		ANA-GND
BLUE	3		13	HSYNC
		9		VCC
NC	4		14	VSYNC
		10		DIG-GND
DIG-GND	5		15	DDCCLK

3.6.32 Signal Description – CRT Connector (CN14)

HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ù cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ù cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ù cable impedance.
DIG-GND	Ground reference for HSYNC and VSYNC.
ANA-GND	Ground reference for RED, GREEN, and BLUE.

3.6.33 Keyboard and PS/2 Mouse Connector (CN15)



3.6.34 Signal Description – Keyboard & PS/2 Mouse Connectors (CN15)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.
MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

3.6.35 10/100BASE-Tx Ethernet Connector (CN16, CN17)

Signal	PIN
TXD+	1
TXD-	2
RXD+	3
NC	4
NC	5
RXD-	6
NC	7
NC	8

3.6.36 Signal Description – 10/100Base-Tx Ethernet Connector (CN16, CN17)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

3.6.37 CD-ROM Audio Input Connector (J5)

Signal	PIN
CD_R	4
CD_GND	3
CD_L	2
CD_GND	1

3.6.38 Signal Configuration – CD-ROM Audio Input Connector (J5)

CD L/R	Left and right CD audio input lines.
CD_GND	GND for left and right CD. This GND level is not connected to the board GND.

3.6.39 Auxiliary Power Connector (PWR1)

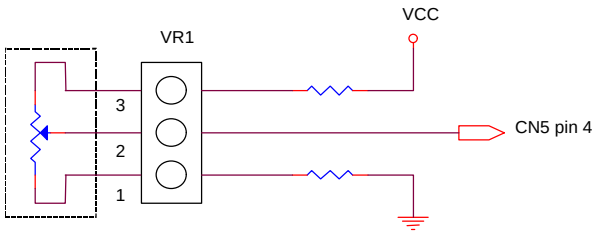
Signal	PIN
-5V	1
GND	2
GND	3
-12V	4

3.6.40 Power Connector (PWR2)

Signal	PIN
VCC	4
GND	3
GND	2
12V	1

3.6.41 LCD Backlight Brightness Adjustment Connector (VR1)

Signal	PIN
VCC	3
VR	2
GND	1



Variation Resistor (Recommended: 4.7K , >1/16W)

4. AWARD BIOS Setup

4.1 Starting Setup

The Award BIOS is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

```
Press DEL to enter SETUP
```

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

```
Press F1 To Continue, DEL to enter SETUP
```

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

4.3 Getting Help

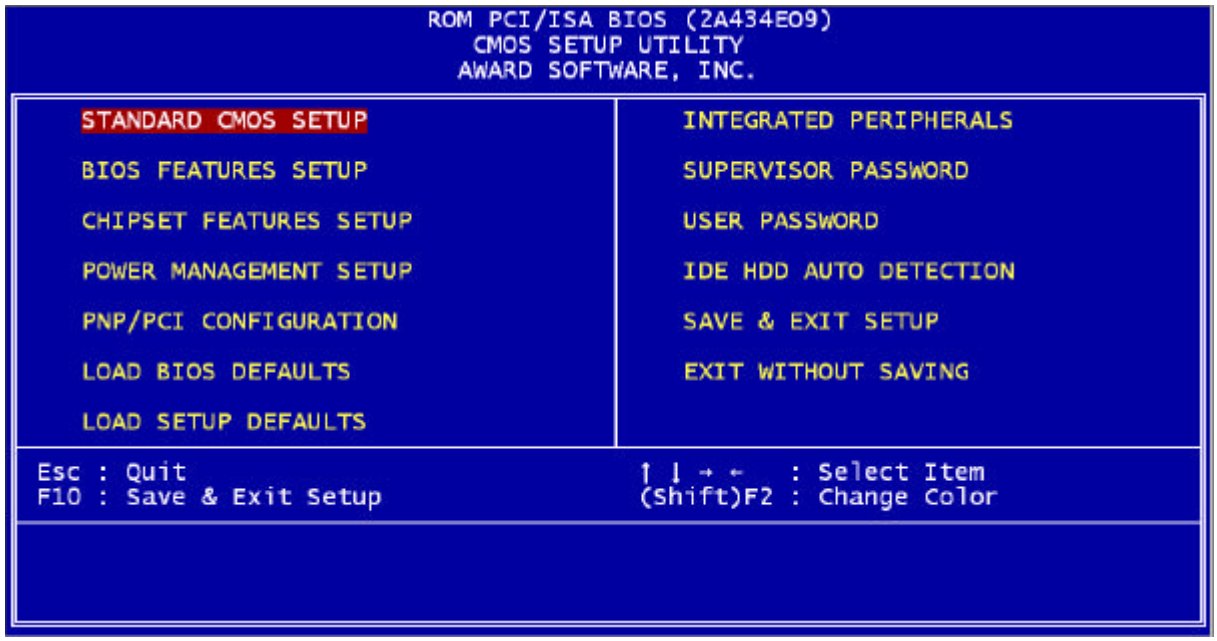
Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

4.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the Award BIOS supports an override to the CMOS settings, which resets your system to its defaults.

4.5 Main Menu

Once you enter the Award BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.



4.5.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

4.5.1.1 Standard CMOS Setup

This setup page includes all the items in a standard, AT-compatible BIOS.

4.5.1.2 BIOS Features Setup

This setup page includes all the items of Award special enhanced features.

4.5.1.3 Super / User Password Setting

Change, set, or disable password. It allows you to limit access to the system and Setup, or just to Setup.

4.5.1.4 Chipset Features Setup

This setup page includes all the items of chipset special features.

4.5.1.5 Power Management Setup

This entry only appears if your system supports Power Management, “Green PC”, standards.

4.5.1.6 PNP / PCI Configuration Setup

This entry appears if your system supports PNP / PCI.

4.5.1.7 Load BIOS Defaults

The BIOS defaults have been set by BCM and represent set to provide the minimum requirements for your system to operate.

4.5.1.8 Load Setup Defaults

The chipset defaults are set to provide for maximum system performance. While Award has designed the custom BIOS to maximize performance, the manufacturer has the right to change these defaults to meet their needs.

4.5.1.9 Integrated Peripherals

This section page includes all the items of IDE hard drive and Programmed Input / Output features.

4.5.1.10 IDE HDD Auto Detection

Automatically detect and configure hard disk parameters. The Award BIOS includes this ability in the event you are uncertain of your hard disk’s parameters.

4.5.1.11 Save & Exit Setup

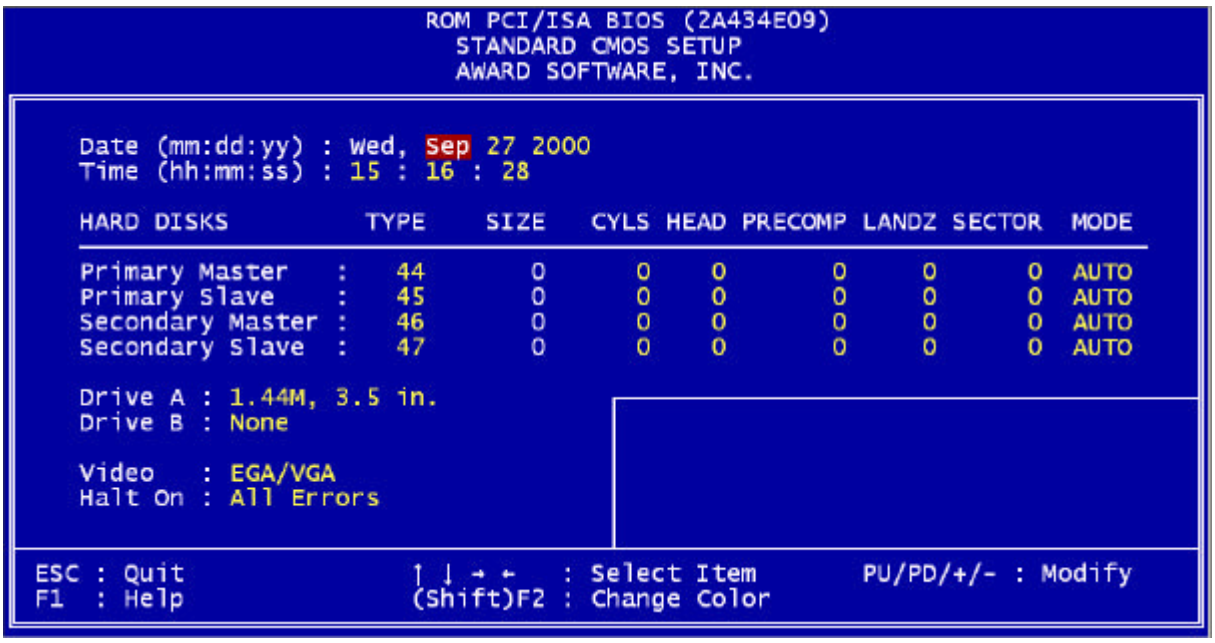
Save CMOS value changes to CMOS and exit setup.

4.5.1.12 Exit Without Save

Abandon all CMOS value changes and exit setup.

4.5.2 Standard CMOS Setup

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.



4.5.2.1 Date

The date format is <day>, <date> <month> <year>. Press <F3> to show the calendar.

day	The day, from Sun to Sat, determined by the BIOS and is display-only
date	The date, from 1 to 31 (or the maximum allowed in the month)
month	The month, Jan through Dec.
year	The year, from 1900 through 2099

4.5.2.2 Time

The time format is <hour> <minute> <second>. The time is calculated based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00.

4.5.2.3 Daylight Saving

The category adds one hour to the clock when daylight-saving time begins. It also subtracts one hour when standard time returns.

Enabled	Enable daylight-saving
Disabled	Disable daylight-saving

4.5.2.4 Primary Master/Primary Slave/Secondary Master/Secondary Slave

The categories identify the types of 2 channels that have been installed in the computer. There are 45 predefined types and 4 users definable types are for Enhanced IDE BIOS. Type 1 to Type 45 are predefined. Type user is user-definable.

Press PgUp or PgDn to select a numbered hard disk type or type the number and press <Enter>. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this category. If your hard disk drive type is not matched or listed, you can use Type "User" to define your own drive type manually.

If you select Type "User", you will need to know the information listed below. Enter the information directly from the keyboard and press <Enter>. This information should be included in the documentation from your hard disk vendor or the system manufacturer.

If the controller of HDD interface is ESDI, the selection shall be "Type 1".

If the controller of HDD interface is SCSI, the selection shall be "None".

If you select Type "Auto", BIOS will Auto-Detect the HDD & CD-ROM Drive at the POST stage and showing the IDE for HDD & CD-ROM Drive.

TYPE	drive type
CYLS.	number of cylinders
HEADS	number of heads
PRECOMP	write precomp
LANDZONE	landing zone
SECTORS	number of sectors
MODE	mode type

If a hard disk has not been installed select NONE and press <Enter>.

4.5.2.5 Drive A Type / Drive B Type

The category identifies the types of floppy disk drive A or drive B that have been installed in the computer.

None	No floppy drive installed
360K, 5.25 in	5-1/4 inch PC-type standard drive; 360 kilobyte capacity
1.2M, 5.25 in	5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
720K, 3.5 in	3-1/2 inch double-sided drive; 720 kilobyte capacity
1.44M, 3.5 in	3-1/2 inch double-sided drive; 1.44 megabyte capacity
2.88M, 3.5 in	3-1/2 inch double-sided drive; 2.88 megabyte capacity

4.5.2.6 Video

The category selects the type of video adapter used for the primary system monitor. Although secondary monitors are supported, you do not have to select the type in Setup.

EGA/VGA	Enhanced Graphics Adapter/Video Graphics Array. For EGA, VGA, SEGA, SVGA or PGA monitor adapters.
CGA 40	Color Graphics Adapter, power up in 40 column mode
CGA 80	Color Graphics Adapter, power up in 80 column mode
MONO	Monochrome adapter, includes high resolution monochrome adapters

4.5.2.7 Halt On

The category determines whether the computer will stop if an error is detected during power up.

No errors	The system boot will not be stopped for any error that may be detected.
All errors	Whenever the BIOS detect a non-fatal error the system will be stopped and you will be prompted.
All, But Keyboard	The system boot will not stop for a keyboard error; it will stop for all other errors.
All, But Diskette	The system boot will not stop for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not stop for a keyboard or disk error; it will stop for all other errors.

4.5.2.8 Memory

The category is display-only which is determined by POST (Power On Self Test) of the BIOS.

4.5.2.9 Base Memory

The POST will determine the amount of base (or conventional) memory installed in the system. The value of the base memory is typically 512K for systems with 512K memory installed on the SBC, or 640K for systems with 640K or more memory installed on the SBC.

4.5.2.10 Extended Memory

The BIOS determines how much extended memory is present during the POST. This is the amount of memory located above 1MB in the CPU's memory address map.

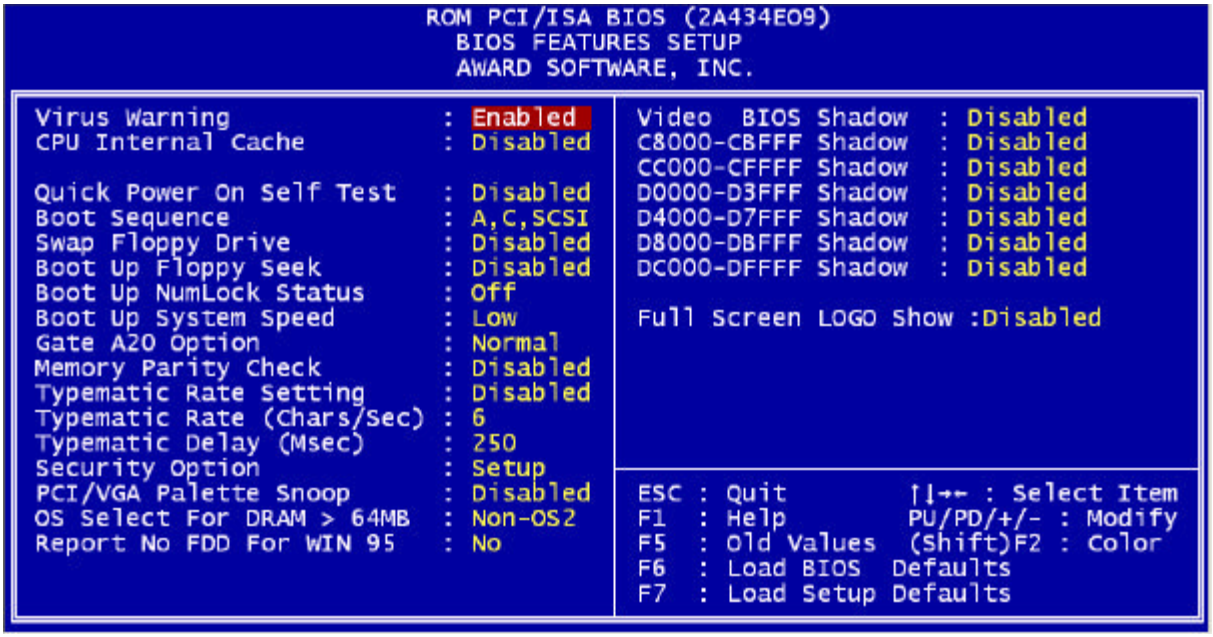
4.5.2.11 Other Memory

This refers to the memory located in the 640K to 1024K address space. This is memory that can be used for different applications. DOS uses this area to load device drivers in an

effort to keep as much base memory free for application programs. The BIOS is the most frequent user of this RAM area since this is where it shadows RAM.

4.5.3 BIOS Features Setup

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



4.5.3.1 Virus Warning

When this item is enabled, the Award BIOS will monitor the boot sector and partition table of the hard disk drive for any attempt at modification. If an attempt is made, the BIOS will halt the system and the following error message will appear. Afterwards, if necessary, you will be able to run an anti-virus program to locate and remove the problem before any damage is done.

> ! WARNING !
>
> Disk boot sector is to be modified
>
> Type "Y" to accept write or "N" to abort write
>
> Award Software, Inc.

4.5.3.2 CPU Internal Cache

This category speeds up memory access. However, it depends on CPU/chipset design. The default value is en able.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.3 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

4.5.3.4 Boot Sequence

This category determines which drive to search first for the disk operating system (i.e., DOS). Default value is A, C.

C, A	System will first search for hard disk drive then floppy disk drive.
A, C	System will first search for floppy disk drive then hard disk drive.
CDROM, C, A	System will first search for CDROM drive, then hard disk drive and the next is floppy disk drive.
C, CDROM, A	System will first search for hard disk drive, then CDROM drive, and the next is floppy disk drive.

4.5.3.5 Swap Floppy Drive

This item allows you to determine whether enable the swap floppy drive or not.

The choice: Enabled/Disabled.

4.5.3.6 Boot Up Floppy Seek

During POST, BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. 360K type is 40 tracks while 760K, 1.2M and 1.44M are all 80 tracks.

Enabled	BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks. Note that BIOS cannot tell from 720K, 1.2M or 1.44M drive type as they are all 80 tracks.
Disabled	BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

4.5.3.7 Boot Up NumLock Status

This allows you to determine the default state of the numeric keypad. By default, the system boots up with NumLock on.

On	Keypad is number keys
Off	Keypad is arrow keys

4.5.3.8 Boot Up System Speed

Selects the default system speed -- the normal operating speed at power up.

High	Set the speed to high
Low	Set the speed to low

4.5.3.9 Gate A20 Option

This entry allows you to select how the gate A20 is handled. The gate A20 is a device used to address memory above 1 Mbytes. Initially, the gate A20 was handled via a pin on the keyboard. Today, while keyboards still provide this support, it is more common, and much faster, for the system chipset to provide support for gate A20.

Normal	keyboard
Fast	chipset

4.5.3.10 Typematic Rate Setting

This determines if the typematic rate is to be used. When disabled, continually holding down a key on your keyboard will generate only one instance. In other words, the BIOS will only report that the key is down. When the typematic rate is enabled, the BIOS will report as before, but it will then wait a moment, and, if the key is still down, it will begin the report that the key has been depressed repeatedly. For example, you would use such a feature to accelerate cursor movements with the arrow keys.

Enabled	Enable typematic rate
Disabled	Disable typematic rate

4.5.3.11 Typematic Rate (Chars/Sec)

When the typematic rate is enabled, this selection allows you select the rate at which the keys are accelerated.

6	6 characters per second
8	8 characters per second
10	10 characters per second
12	12 characters per second
15	15 characters per second
20	20 characters per second
24	24 characters per second
30	30 characters per second

4.5.3.12 Typematic Delay (Msec)

When the typematic rate is enabled, this selection allows you to select the delay between when the key was first depressed and when the acceleration begins.

250	250 msec
500	500 msec
750	750 msec
1000	1000 msec

4.5.3.13 Security Option

This category allows you to limit access to the system and Setup, or just to Setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

4.5.3.14 PCI / VGA Palette Snoop

It determines whether the MPEG ISA/VESA VGA Cards can work with PCI/VGA or not.

Enabled	When PCI/VGA working with MPEG ISA/VESA VGA Card.
Disabled	When PCI/VGA not working with MPEG ISA/VESA VGA Card.

4.5.3.15 OS Select for DRAM > 64

This item allows you to access the memory that over 64MB in OS/2.

The choice: Non-OS2, OS2.

4.5.3.16 Report No FDD for WIN95

4.5.3.17 Video BIOS Shadow

Determines whether video BIOS will be copied to RAM. However, it is optional depending on chipset design. Video Shadow will increase the video speed.

Enabled	Video shadow is enabled
Disabled	Video shadow is disabled

4.5.3.18 C8000 – CBFFF Shadow/DC000 – DFFFF Shadow

These categories determine whether option ROMs will be copied to RAM. An example of such option ROM would be support of on-board SCSI.

Enabled	Optional shadow is enabled
Disabled	Optional shadow is disabled

4.5.3.19 Full Screen Logo Show

4.5.4 Supervisor/User Password Setting

You can set either supervisor or user password, or both of then. The differences between are:

supervisor password: can enter and change the options of the setup menus.

user password: just can only enter but do not have the right to change the options of the setup menus.

When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

```
ENTER PASSWORD:
```

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

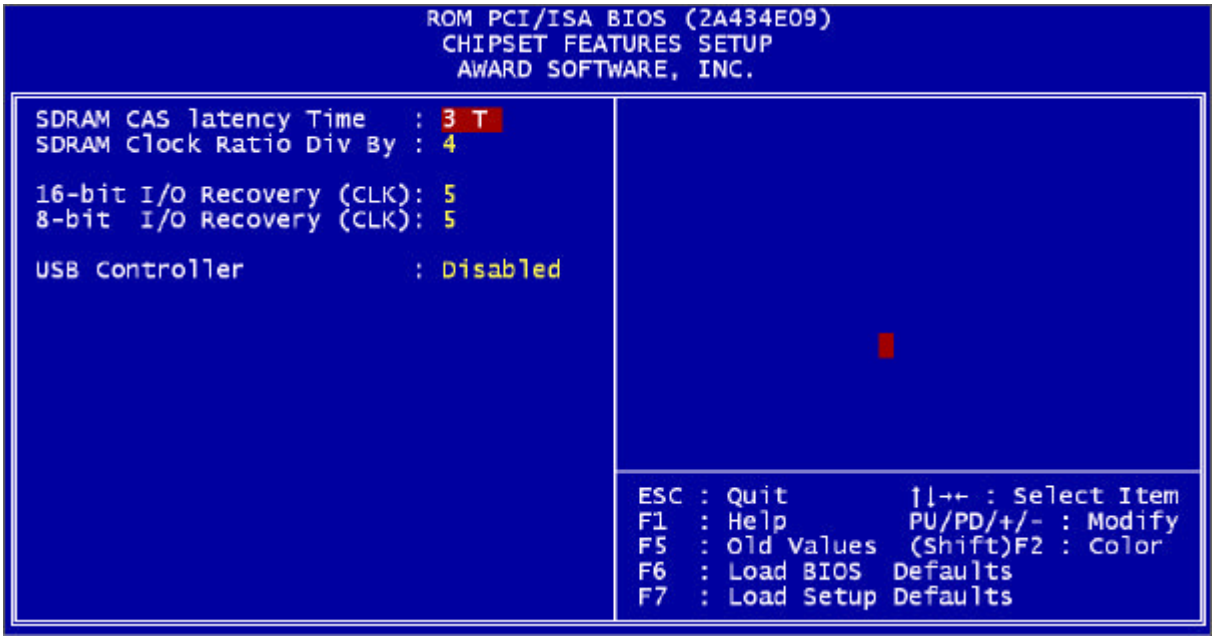
```
PASSWORD DISABLED.
```

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup.

4.5.5 Chipset Setup



ADVANCED OPTIONS. The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

4.5.5.1 SDRAM CAS Latency Time

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.

The choice: Auto, 2T, 3T.

4.5.5.2 SDRAM Clock Ratio Div By

This item allows user to set the DRAM timing.

4.5.5.3 16-bit I/O Recovery (CLK)

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

The choice: from 1 to 16 CPU clocks.

4.5.5.4 8-bit I/O Recovery (CLK)

The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is so much faster than the ISA bus.

This item allows you to determine the recovery time allowed for 8-bit I/O.

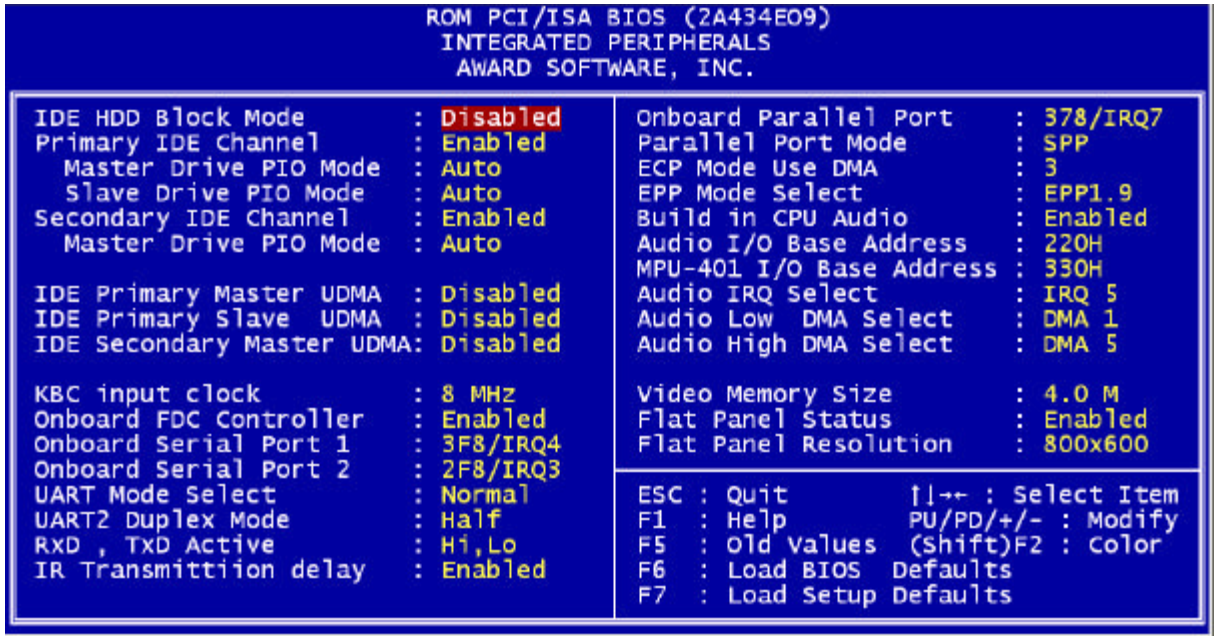
The choice: from 1 to 16 CPU clocks.

4.5.5.5 USB Controller / USB Legacy Support

Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

The choice: Enabled, Disabled.

4.5.6 Integrated Peripherals Features Setup



4.5.6.1 IDE HDD Block Mode

This allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive (HDD).

Enabled	IDE controller uses block mode.
Disabled	IDE controller uses standard mode.

4.5.6.2 Primary/Secondary IDE Channel

You may separately disable the primary/second channel on an IDE interface installed in a PCI expansion slot.

4.5.6.3 IDE Primary/Secondary Master/Slave PIO Mode

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports.

Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

4.5.6.4 IDE Primary/Secondary Master/Slave UDMA

This item allows you to enable/disable the IDE Primary/Secondary Master / Slave UDMA mode.

The Choice: Auto, Disabled

4.5.6.5 KBC Input Clock

This item allows you to select the KBC input clock frequency.

The Choice: 6MHz, 8MHz, 12MHz, 16MHz.

4.5.6.6 Onboard FDD Controller

This should be enabled if your system has a floppy disk drive (FDD) installed on the system board and you wish to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature.

The Choice: Enabled, Disabled.

4.5.6.7 Onboard Serial Port 1/Port 2

This item allows you to determine access onboard serial port 1/port 2 controller with which I/O address.

The Choice: 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Disabled, Auto.

4.5.6.8 UART Mode Select

This item allows you to determine which Infra Red (IR) function of onboard I/O chip.

The Choice: IrDA, ASKIR, Normal.

4.5.6.9 UART2 Duplex Mode

Select the value required by the IR device connected to the IR port. Full-duplex mode permits simultaneous two-direction transmission. Half-duplex mode permits transmission in one direction only at a time.

The Choice: Half, Full.

4.5.6.10 RxD, TxD Active

This item allows you to determine the active of RxD, TxD.

The Choice: i, Hi", o, Lo", o, Hi", i, Lo".

4.5.6.11 IR Transmission Delay

This item allows you to enable / disable the IR transmission delay.

The Choice: Enabled, Disabled.

4.5.6.12 Onboard Parallel Port

Select a logical LPT port name and matching address for the physical parallel (printer) port.

The choice: 378H/IRQ7, 278H/IRQ5, 3BCH/IRQ7, Disabled.

4.5.6.13 Parallel Port Mode

Select an operating mode for the onboard parallel port. Select Compatible or Extended unless you are certain both your hardware and software support EPP or ECP mode.

The choice: ECP+EPP1.7, EPP1.7+SPP, EPP1.9+SPP, ECP+EPP1.9, ECP, Normal, SPP,.

4.5.6.14 ECP Mode Use DMA

Select a DMA channel for the port.

The choice: 3, 1.

4.5.6.15 EPP Mode Select

Select EPP port type 1.7 or 1.9.

The choice: EPP1.7, EPP1.9.

4.5.6.16 Build in CPU Audio

This item allows you to select the option of the build in CPU Audio function.

The choice: Enable, Disable.

4.5.6.17 Audio I/O Base Address

This chipset traps I/O accesses for Sound Blaster compatibility at 220H, 240H, 260H, or 280H.

The choice: 220H, 240H, 260H, 280H.

4.5.6.18 MPU-401 I/O Base Address

This chipset traps I/O accesses for ROLAND MPU 401 UART interface at 330H, 300H, or Disable.

The choice: 330H, 300H, Disable.

4.5.6.19 Audio IRQ Select

Select an interrupt for the audio port.

The choice: IRQ 9, IRQ 5, IRQ 7, IRQ 10, Disable.

4.5.6.20 Audio Low DMA Select

This chipset supports I/O trapping for low DMA accesses and allows you to select the Audio Low DMA type.

The choice: DMA 0, DMA 1, DMA 3, Disable.

4.5.6.21 Audio High DMA Select

This chipset supports I/O trapping for high DMA accesses and allows you to select the Audio High DMA type.

The choice: DMA 5, DMA 6, DMA 7, Disable.

4.5.6.22 Video Memory Size

Select the Video memory size.

The choice: 1M, 2M, 3M, 4M.

4.5.6.23 Flat Panel Status

This item allows you to select the option of the build in flat panel controller.

The choice: Enable, Disable.

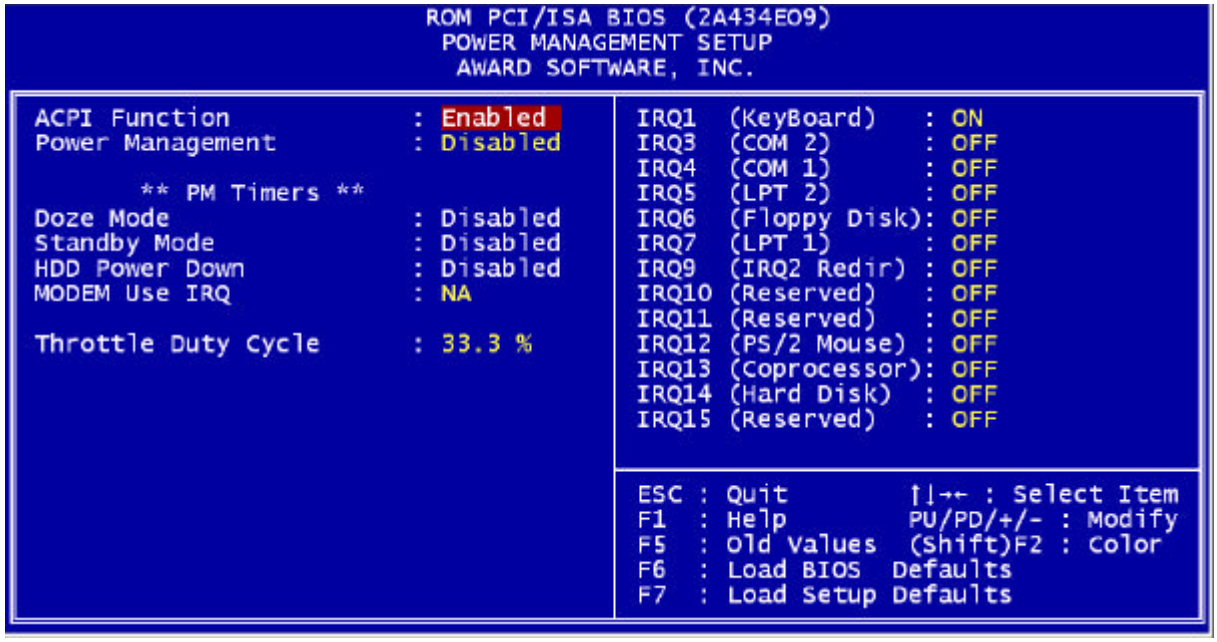
4.5.6.24 Flat Panel Resolution

Select the flat panel resolution.

The choice: 640 x 480, 800 x 600, 1024 x 768.

4.5.7 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



4.5.7.1 ACPI Function

This item allows you to select the option of the ACPI power management function.

The choice: Enable, Disable.

4.5.7.2 Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

1. Doze Mode
2. Standby Mode
3. HDD Power Down

There are four selections for Power Management, three of which have fixed mode settings.

Disable (default)	No power management. Disables all four modes
Min. Power Saving	Minimum power management. Doze Mode = 1 hr. Standby Mode = 1 hr., Suspend Mode = 1 hr., and HDD Power Down = 15 min.
Max. Power Saving	Maximum power management -- **ONLY AVAILABLE FOR SL CPU's**. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min., and HDD Power Down = 1 min.
User Defined	Allow you to set each mode individually. When not disabled, each of the ranges is from 1 min. to 1 hr. except for HDD Power Down. Ranges from 1 min. to 15 min. and disable.

4.5.7.3 PM Timers

The following four modes are Green PC powers saving functions are only user configurable when *User Defined* Power Management has been selected. See above for available selections.

4.5.7.3.1 Doze Mode

When enabled and after the set time of system inactivity, the CPU clock will run at slower speed while all other devices still operate at full speed.

4.5.7.3.2 Standby Mode

When enabled and after the set time of system inactivity, the fixed disk drive and the video would be shut off while all other devices still operate at full speed.

4.5.7.3.3 HDD Power Down

When enabled and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.

4.5.7.3.4 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choice: 3, 4, 5, 7, 9, 10, 11, NA.

4.5.7.3.5 Throttle Duty Cycle

Select the throttle duty cycle.

The choice: 12.5%, 33.3%, 50%, 75%.

4.5.7.4 Power Down & Resume Events

Power Down and Resume events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode. In effect, the system remains alert for anything occurs to a device configured as *on*, even when the system is in a power down mode.

The following is a list of IRQ's, **I**nterrupt **R**e**Q**uests, which can be exempted much as the COM ports and LPT ports above can. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service.

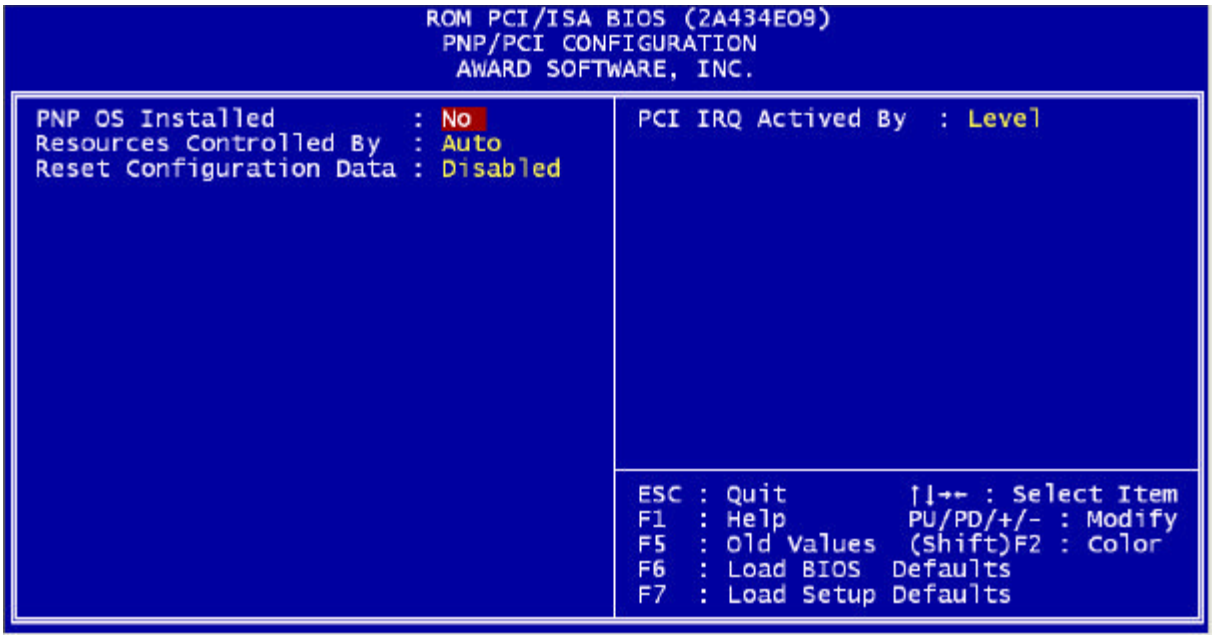
As above, the choices are *On* and *Off.* *Off* is the default.

When set *Off*, activity will neither prevent the system from going into a power management mode nor awaken it.

- IRQ1 (Keyboard)
- IRQ3 (COM 2)
- IRQ4 (COM1)
- IRQ5 (LPT 2)
- IRQ6 (Floppy Disk)
- IRQ7 (LPT 1)
- IRQ9 (IRQ2 Redir)
- IRQ10 (Reserved)
- IRQ11 (Reserved)
- IRQ12 (PS/2 Mouse)
- IRQ13 (Coprocessor)
- IRQ14 (Hard Disk)
- IRQ15 (Reserved)

4.5.8 PnP/PCI Configuration Setup

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system that allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



4.5.8.1 PnP OS Installed

This determines whether the PnP OS is installed or not.

Choices are *Yes* and *No*.

4.5.8.2 Resource Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows® 95.

Choices are *Auto* and *Manual*.

4.5.8.3 Reset Configuration Data

This item allows you to determine reset the configuration data or not.

Choices are *Enabled* and *Disabled*.

4.5.8.4 IRQ - *X* / DMA – *X* Assigned To

This item allows you to determine the IRQ / DMA assigned to the ISA bus and is not available to any PCI slot.

Choices are *Legacy ISA* and *PCI/ISA PnP*.

4.5.8.5 PCI IRQ Activated By

This sets the method by which the PCI bus recognizes that an IRQ service is being requested by a device. Under all circumstances, you should retain the default configuration unless advised otherwise by your system's manufacturer.

Choices are *Level* and *Edge*.

4.5.8.6 Used MEM Base Addr

4.5.8.7 Used MEM Length

5. Driver Installation

5.1 Driver installation for Ethernet Adapter

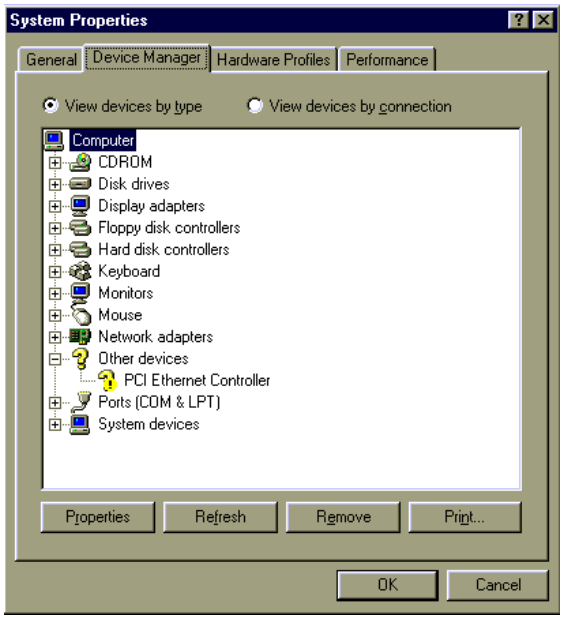
5.1.1 Windows 9x

The following procedures illustrate how to install the driver for the Ethernet controller.

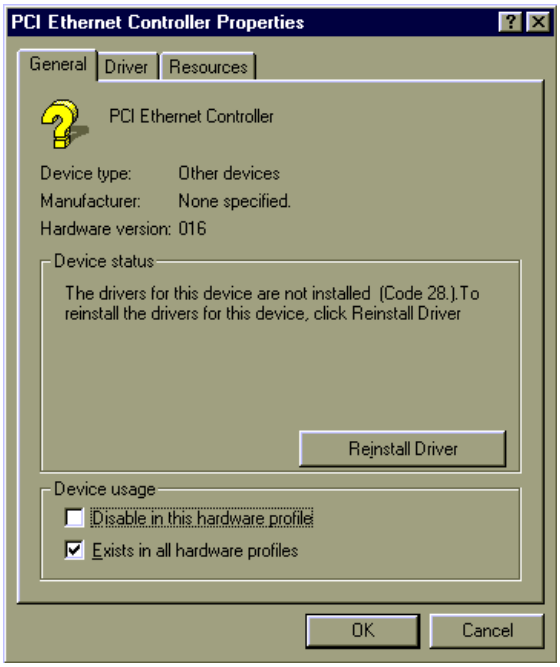
1. Click the '*Start*' button, click on '*Settings*' and on '*Control panel*' to open the control panel. Your display should now look as below (possibly with different size and icons):

2. Double click the '*System*' icon (highlighted below).

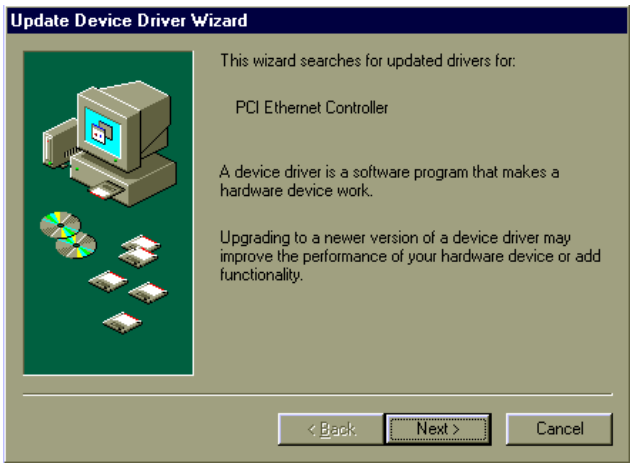
3. Select the '*Device Manager*' tab. If the '*Network adapters'* line is present, expand the line and your screen might look like this:



4. Click the '*Reinstall Driver*' icon to install the driver of Ethernet controller.

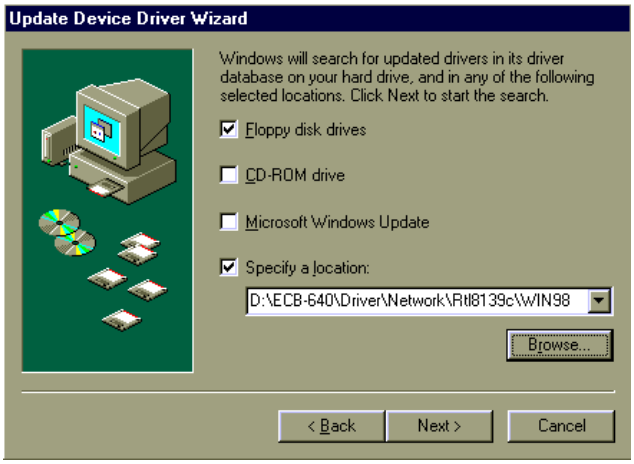


5. Click '*Next*' to continue.



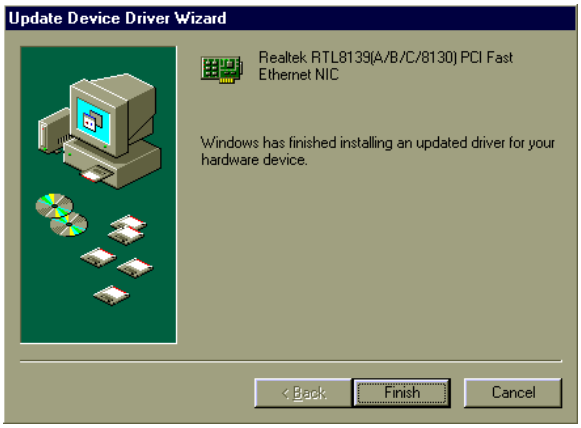
6. Select '*Search for better driver than the one your device is using now*' and Click '*Next*' to continue the driver installation.

7. Specify the location of network adapter driver and click '*Next*' (see below).

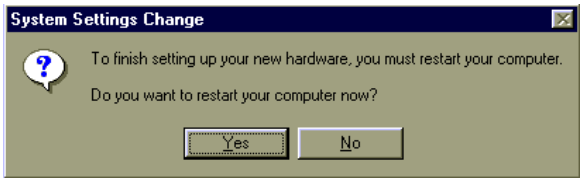


8. Click the '*Next*' button.

9. Click the '*Finish*' button.



10. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.



Further configuration of the adapter may be made in the '*Advanced*' section of the driver properties. These options may be accessed through the '*Network*' icon in the control panel (Select the network adapter, click the '*Properties*' button and select the '*Advanced*' tab).

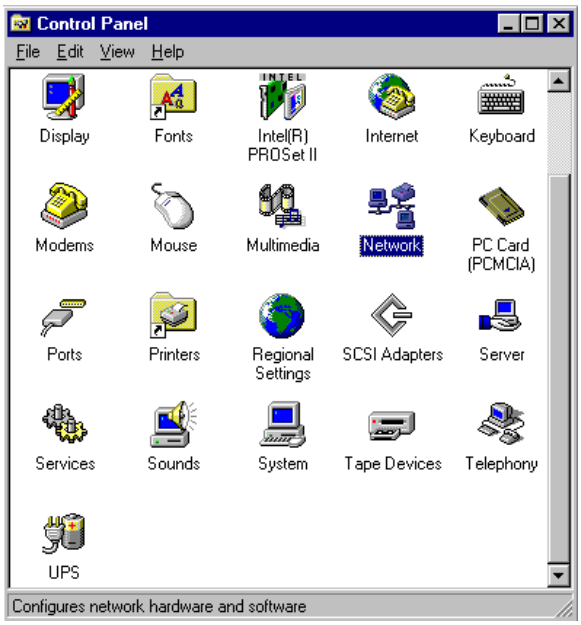
5.1.2 Windows NT 4.0 Ethernet Installation

A driver for the Realtek RTL8139C Ethernet controller on board is included in the attached supporting CD-ROM. The driver for this adapter is denoted 'Realtek RTL8139(A/B/C) PCI Fast Ethernet Adapter'. This driver may be installed in two ways:

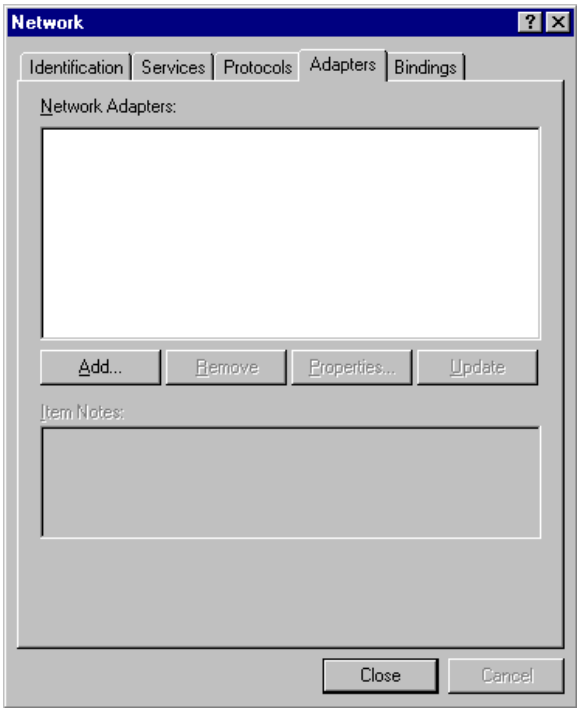
- During the installation process where the network may be configured as an integrated part. In this case the adapter may be chosen or auto-detected when the network adapter is to be installed.
- In the network settings after Windows NT 4.0 is installed.

The following procedures describe the steps to install the Network adapter driver on Windows NT 4.0.

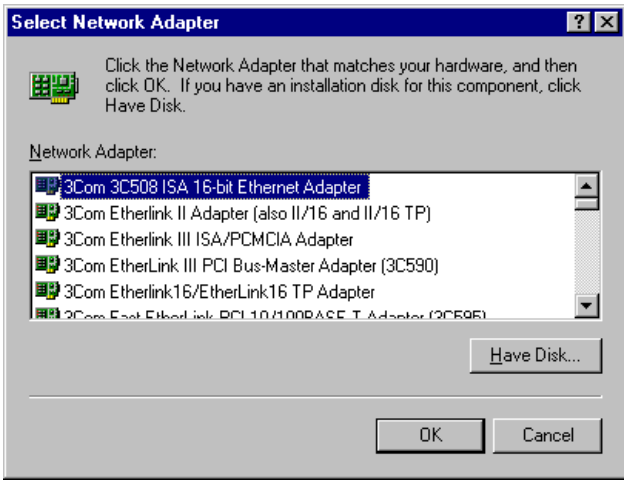
1. Click the '*Start*' button on the task bar. Select '*Settings*' and '*Control Panel*' to start the control panel shown below:



2. Double click the '*Network*' icon and then click the '*Adapters*' tab on the following window. A window as the one shown below should now appear.

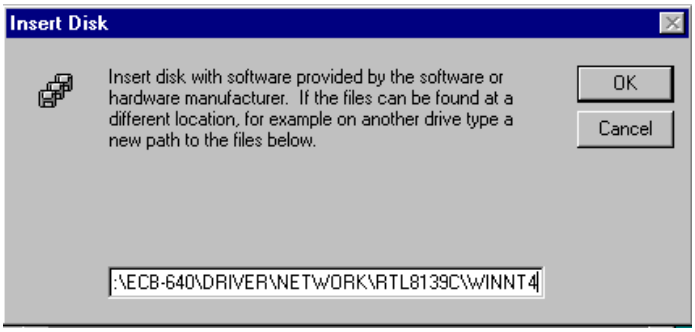


3. Click the '*Add...*' button, and the following window should appear.

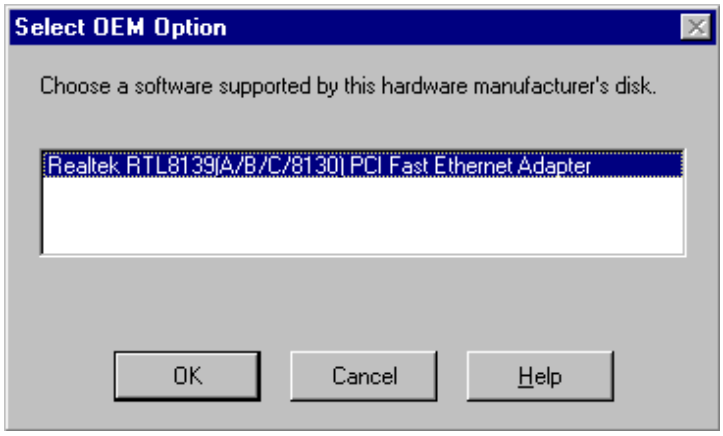


4. Click the '*Have Disk…*' button to install the Network adapter driver from CD-ROM. A window as the one shown below should now appear.

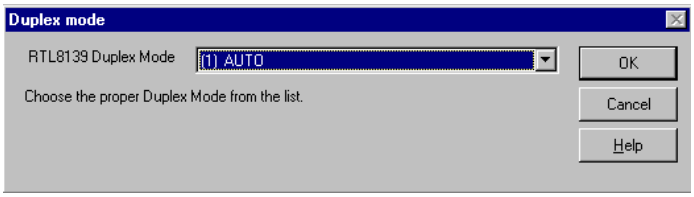
5. Locate the path of Network adapter driver and click the '*OK*' button.



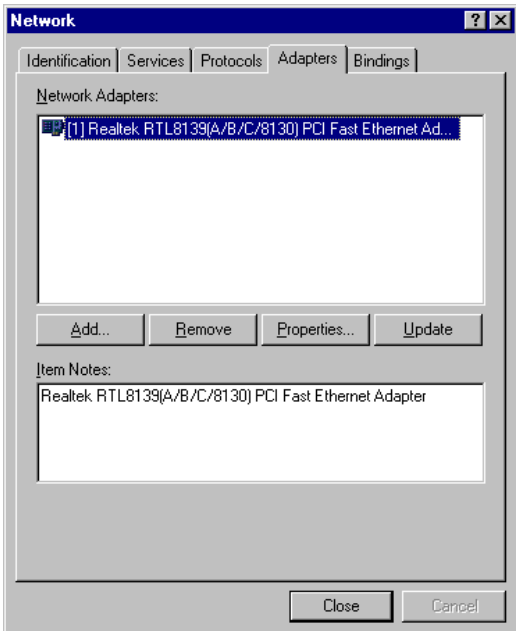
6. Select the '*Realtek RTL8139(A/B/C) PCI Fast Ethernet Adapter*' from the list (as shown below) and click the '*OK*' button.



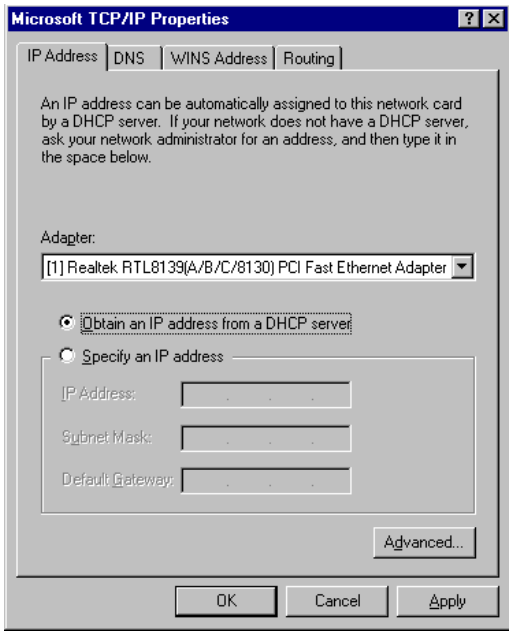
7. Select the '(1) Auto' to set RTL8139C Ethernet controller to Auto Duplex Mode (as shown below) and click the '*OK*' button.



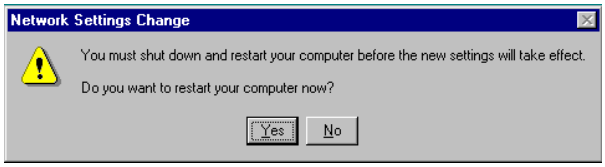
8. Click '*Close*' to accept the settings.



9. Protocols, Services etc. may now be installed and configured for the network to be used. An example is shown below.



10. To complete the installation, reboot the computer by clicking the '*Yes*' button in the window shown below.



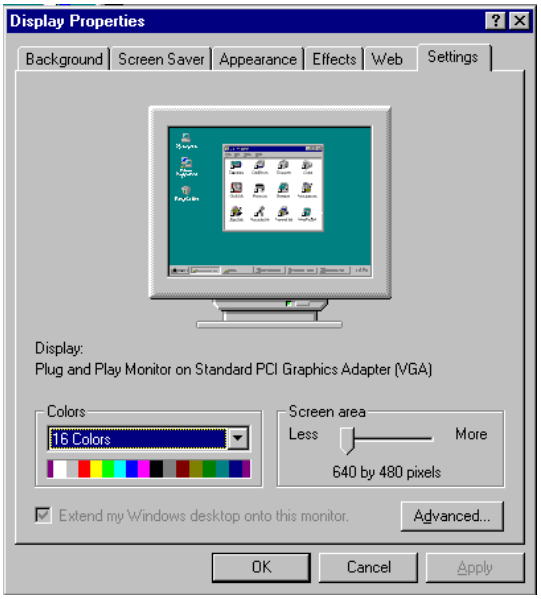
5.2 Driver Installation for Display Adapter

5.2.1 Windows 9x

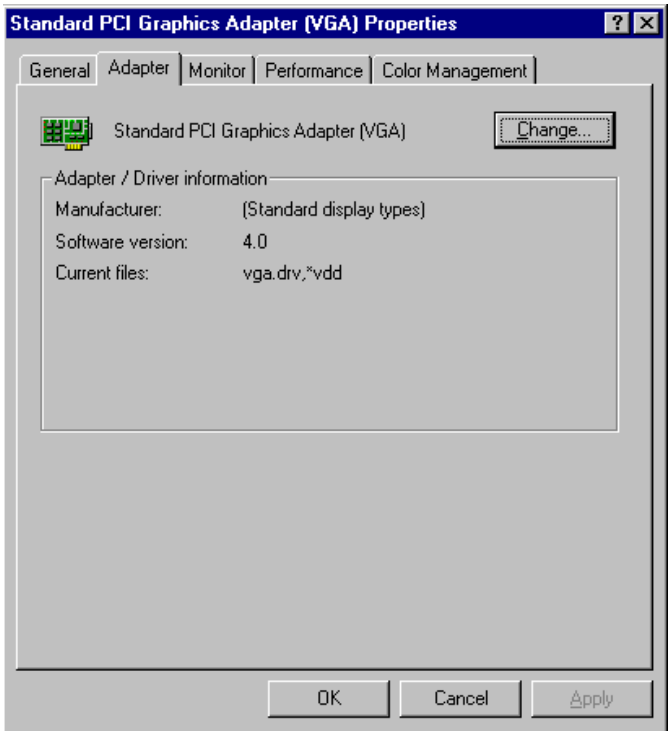
The following steps will install the display driver for the '*National Geode XpressGRAPHICS*' display controller.

1. Click the '*Start*' button on the task bar, select '*Settings*' and '*Control Panel*' from the sub-menu. This should start the Control Panel as shown below:

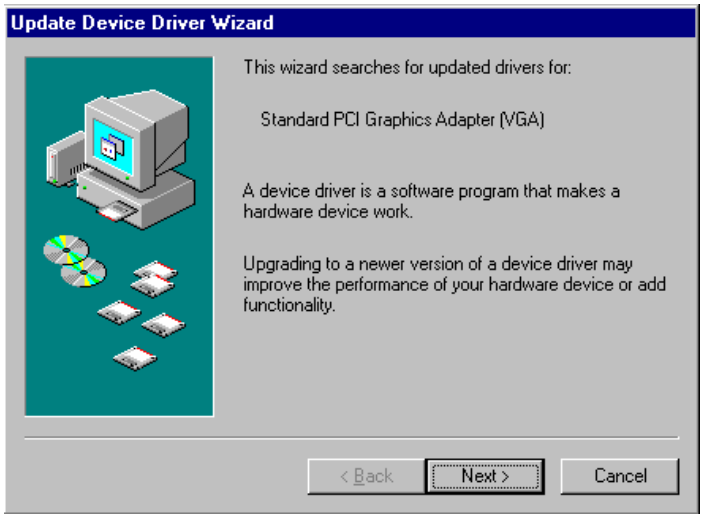
2. Double click the '*Display*' icon and select the '*Settings*' tab as shown below.



3. Click the '*Advanced…*' button. This will show the following window. Click the '*Change…*' button in the Adapter Type frame to select another driver. Your display will probably have another driver then the '*Standard PCI Graphics Adapter (VGA)*' installed at this moment.

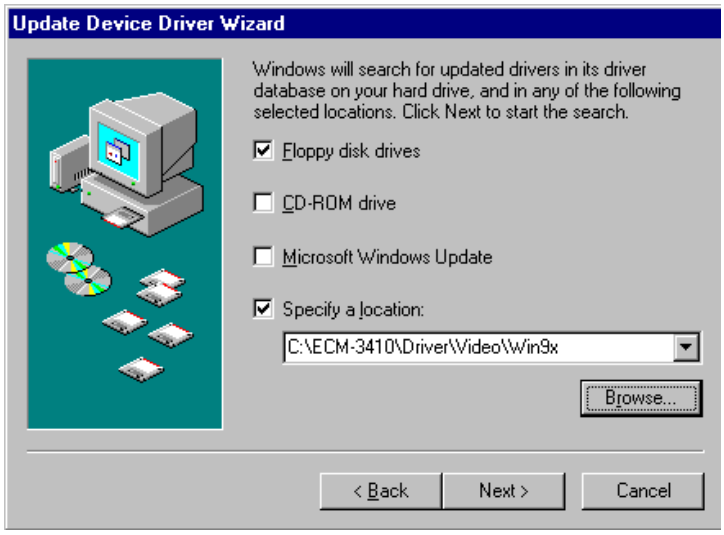


4. Click the '*Next*' to update the display driver.

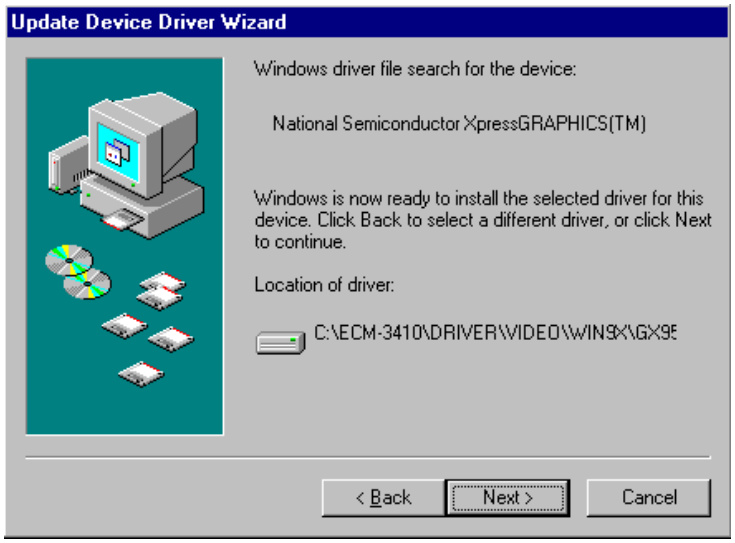


5. Click the '*Next*' to continue the display driver installation.

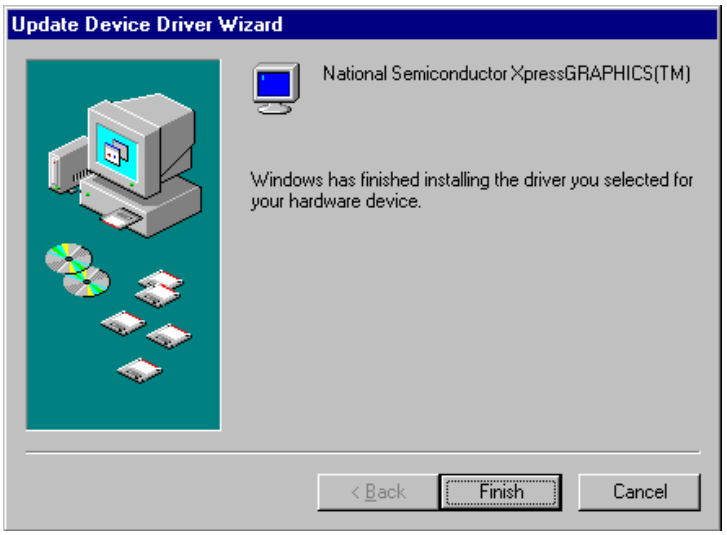
6. Locate the path of Graphics adapter driver and click the '*Next*' button.



7. The driver files will now be read and the display adapter is shown as the following. Click the '*Next*' button to install the display driver.



8. Click the '*Finish*' button.



9. To complete the display driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

10. Further configuration of the display adapter may be made from the '*Display Properties*' window (follow step 1 above). The '*Settings*' tab allows you to change resolution, number of colours etc.

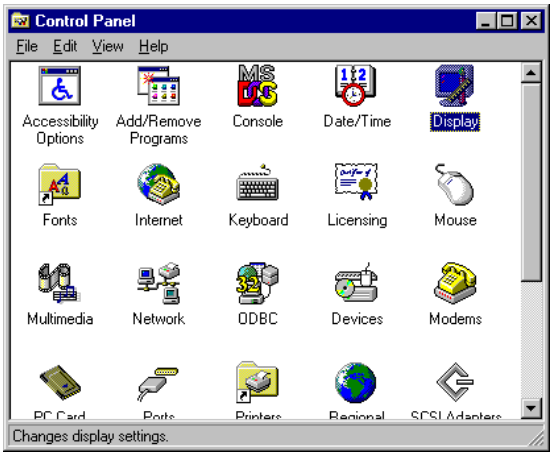
5.2.2 Windows NT 4.0 Display Installation

A display driver for Windows NT 4.0 is supplied with the system on the supporting CD-ROM.

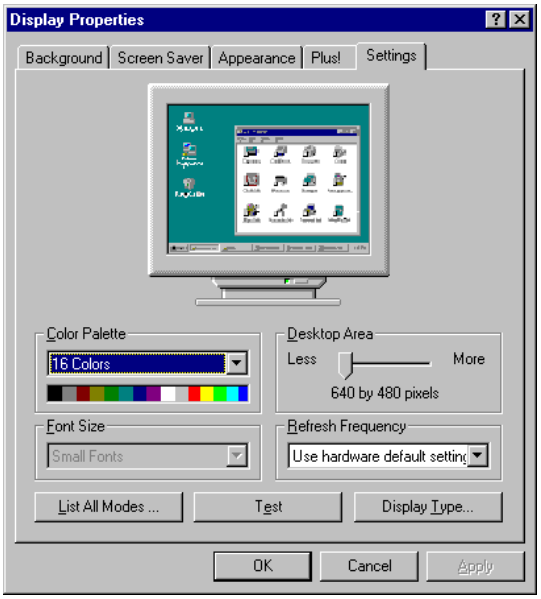
The driver installation may be performed according to the following steps.

1. Start the control panel by clicking the '*Start*' button, click '*Settings*' and '*Control Panel*' from the sub-menu.

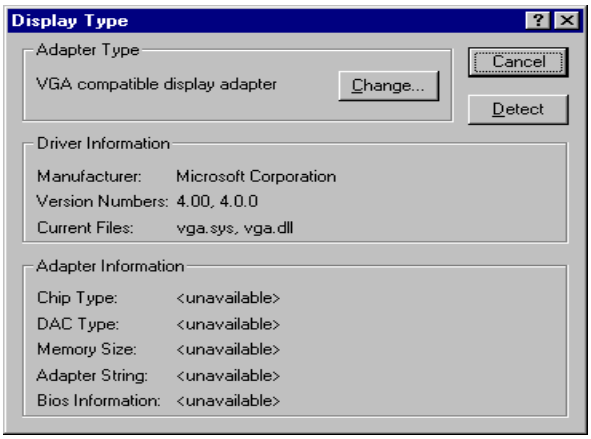
2. Double click the '*Display*' icon in the control panel as shown below:



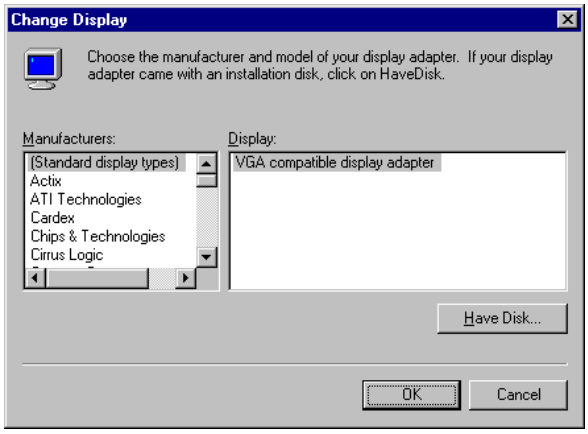
3. On the Display properties window, select the '*Settings*' tab as shown below:



4. Click the '*Display Type*' button and the following window should appear.

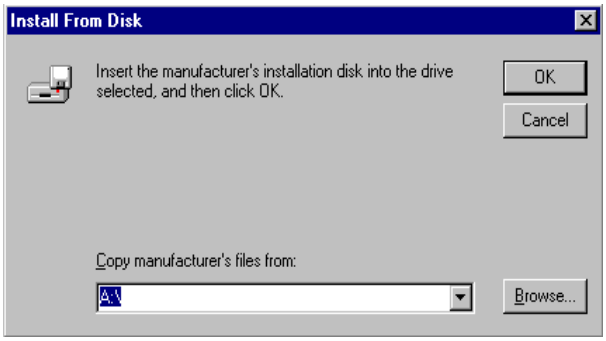


5. Click the '*Change*' button to select another driver. The following window should then appear.

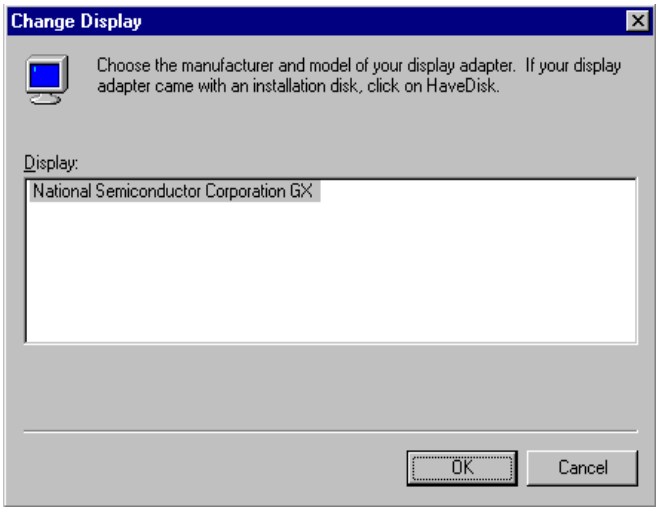


6. Since the driver should be supplied separately, click the '*Have Disk*' button.

7. Insert the attached supporting CD-ROM. The directory for the VGA driver may now be entered.



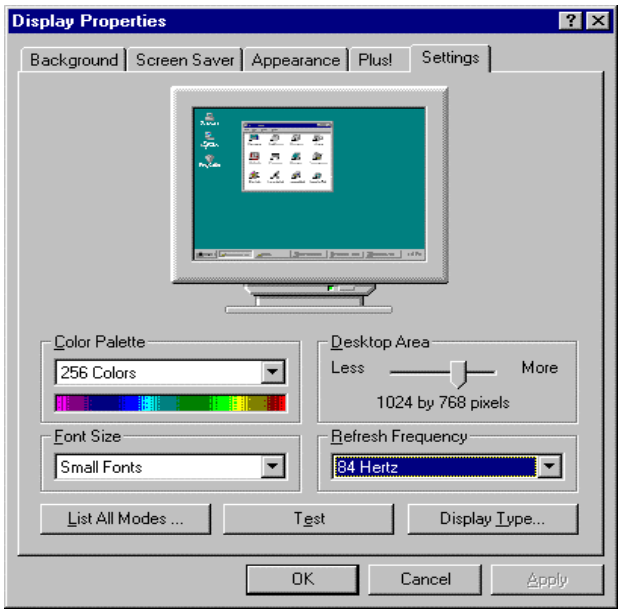
8. The display driver should now be listed as shown below. Click '*OK*' to accept.



9. The driver will now be installed, and the following message should be shown shortly after:

10. Click '*OK*' and close the '*Display Type*' and '*Display Properties*' windows by clicking the '*Close*' button in each window.
11. After closing the '*Display Properties*' window, the computer must be restarted for the changes to take effect.

12. After the reboot, display resolution etc. may be changed in the '*Display Properties*' window (opened by following steps 1 and 2 above). An example is shown below:



13. Before accepting the new settings by pressing '*OK*', a test should be performed by clicking the '*Test*' button.

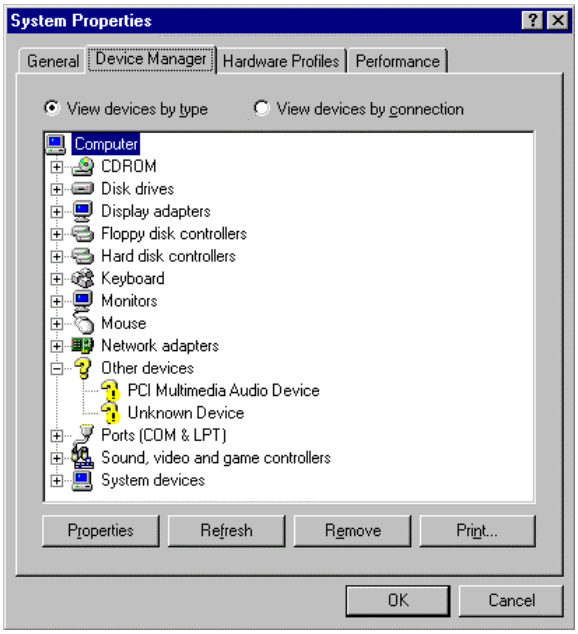
5.3 Driver Installation for Audio Adapter

5.3.1 Windows 9x

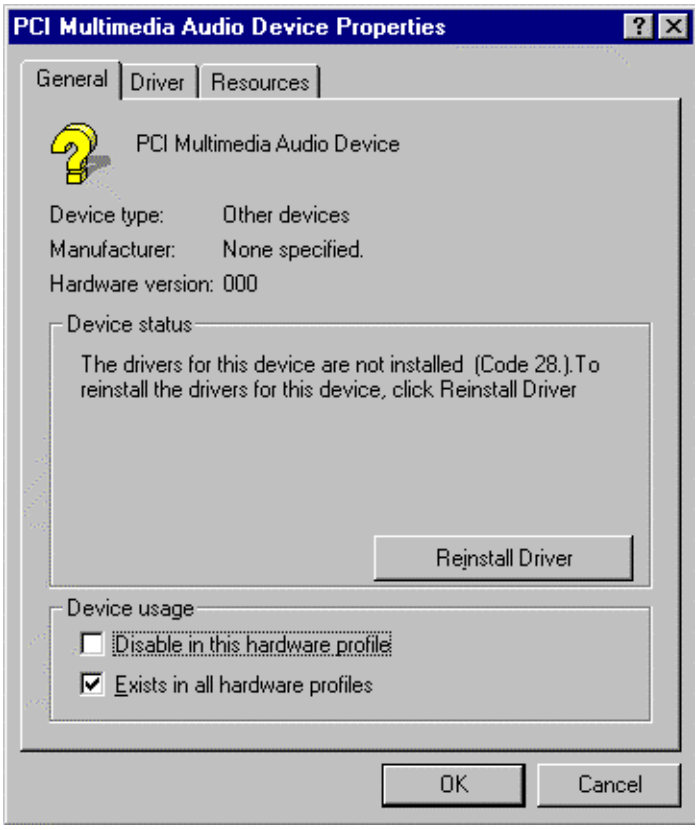
The following steps will install the display driver for the 'National Geode XpressGRAPHICS' display controller.

1. Click the '*Start*' button on the task bar, select '*Settings*' and '*Control Panel*' from the sub-menu. This should start the Control Panel as shown below:

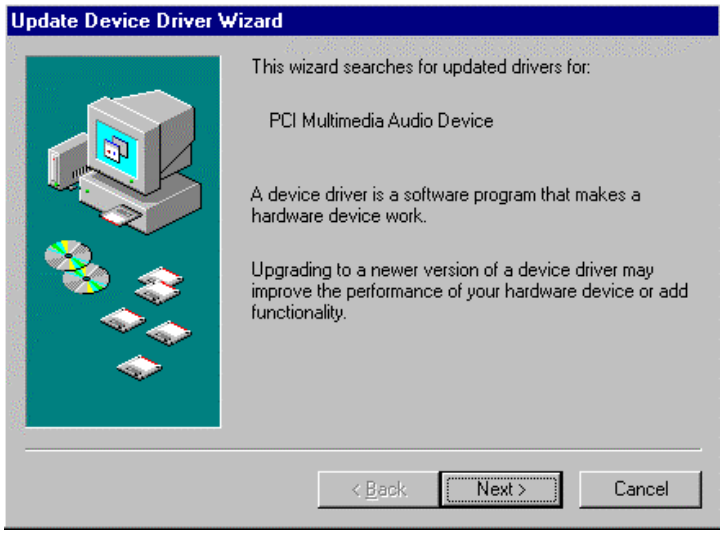
2. Double click the '*System*' icon and select the '*Device Manager*' tab as shown below.



3. Select '*PCI Multimedia Audio Device*'. This will show the following window. Click the '*Reinstall Driver'* button.

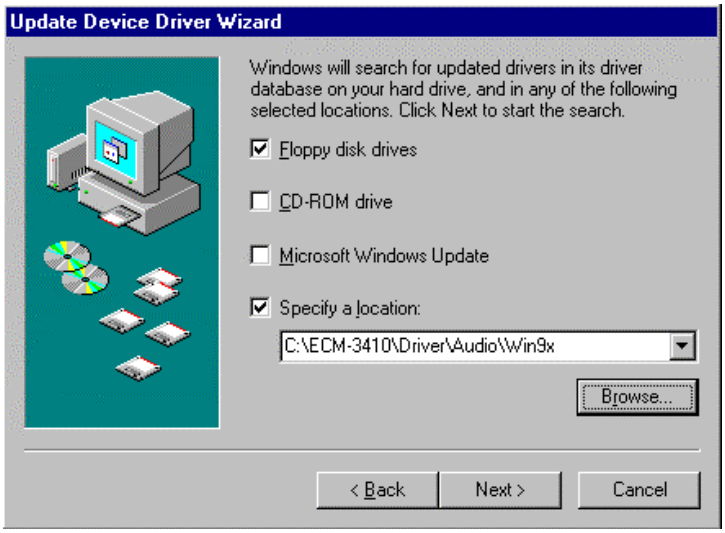


4. Click the '*Next*' to update the audio driver.



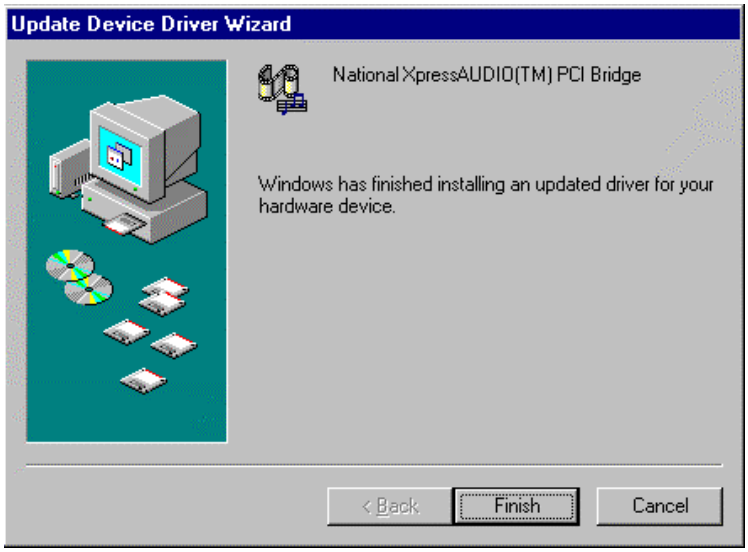
5. Click the '*Next*' to continue the audio driver installation.

6. Locate the path of Audio adapter driver and click the '*Next*' button.

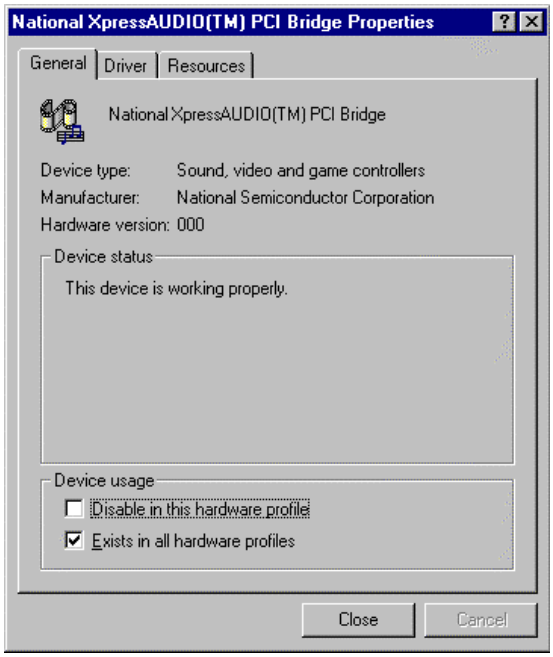


7. The driver files will now be read and the audio adapter is shown as the following. Click the '*Next*' button to install the audio driver.

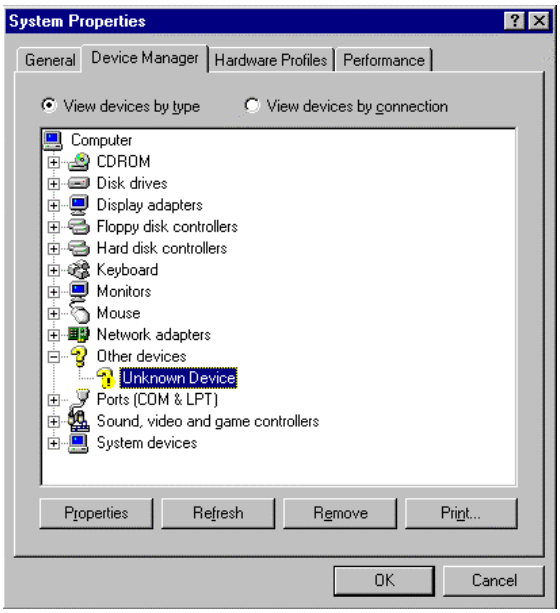
8. Click the '*Finish*' button.



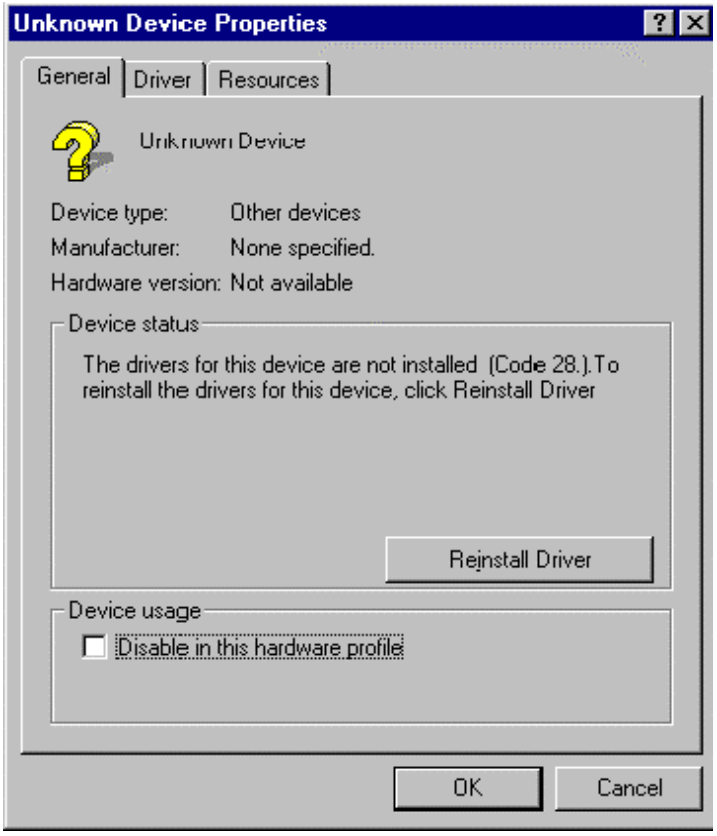
9. Click the '*Close*' button to close the '*National XpressAUDIO PCI Bridge Properties*' window.



10. Select the '*Device Manager*' tab in the '*System Properties*' windows as shown below.

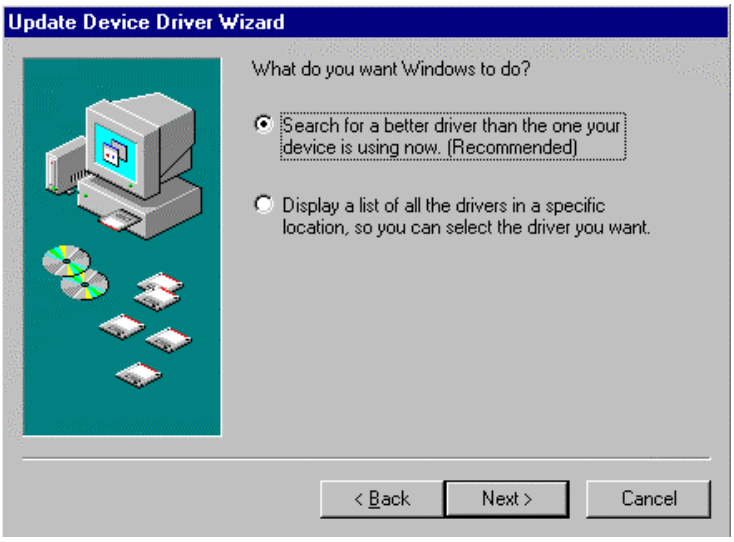


11. Select '*Unknown Device*'. This will show the following window. Click the '*Reinstall Driver'* button.

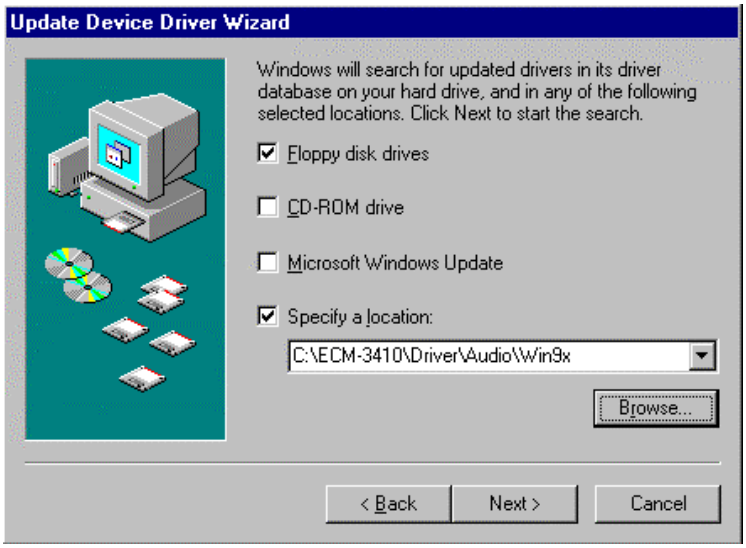


12. Click the '*Next*' to update the audio driver.

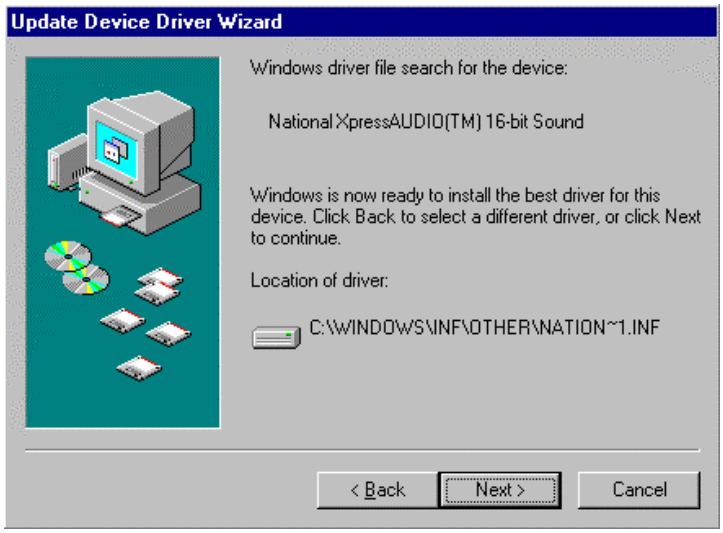
13.Click the '*Next*' to continue the audio driver installation.



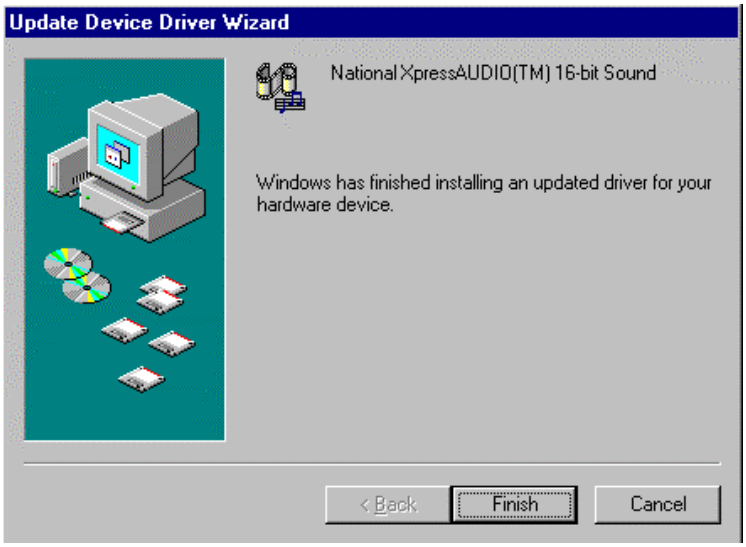
14.Locate the path of Audio adapter driver and click the '*Next*' button.



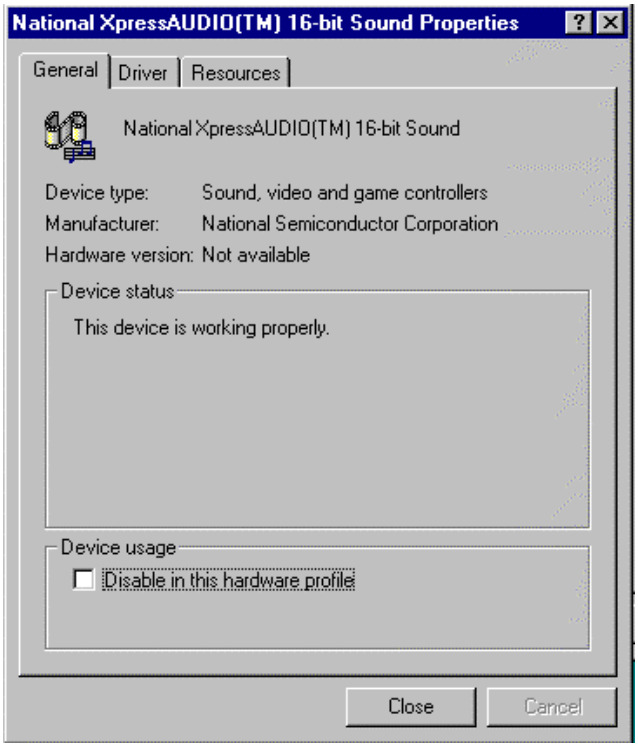
15. The driver files will now be read and the audio adapter is shown as the following. Click the '*Next*' button to install the audio driver.



16. Click the '*Finish*' button.



17. Click the '*Close*' button to close the '*National XpressAUDIO 16-bit Sound Properties*' window.



18. To complete the audio driver installation, reboot the computer by clicking the '*Yes*' button in the window shown below.

5.3.2 Windows NT 4.0 Audio Installation

An audio driver for Windows NT 4.0 is supplied with the system on the supporting CD-ROM.

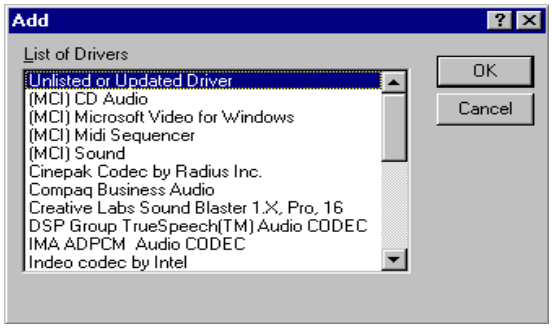
The driver installation may be perform by the following steps:

1. Start the control panel by clicking the '*Start*' button, click '*Settings*' and '*Control Panel*' from the sub-menu.

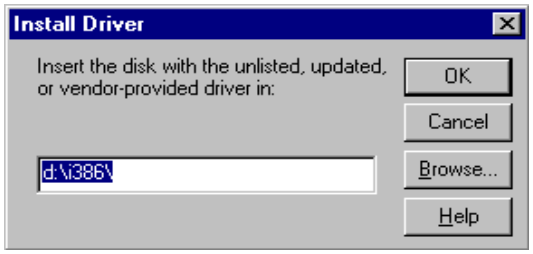
2. Double click the '*Multimedia*' icon in the control panel as shown below:

3. On the Multimedia properties window, select the '*Devices*' tab as shown below:

4. Click the '*Add…*' button and the following window should appear.

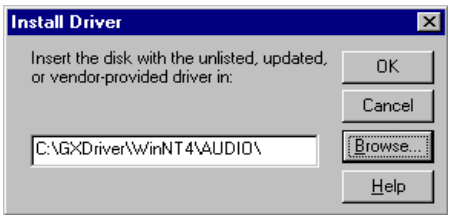


5. Select the '*Unlisted or Updated Driver*' to install the Audio driver from the supporting CD-ROM. The following window should then appear.

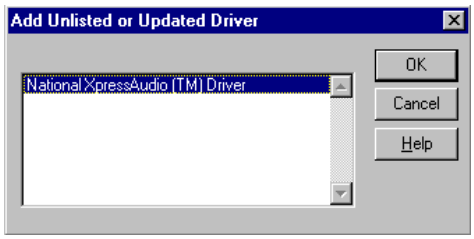


6. Click '*Browse…*' to specify the directory of Audio driver as shown below.

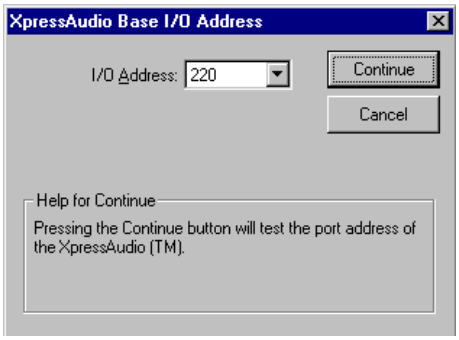
7. Insert the attached supporting CD-ROM. The directory of Audio driver may now be entered.

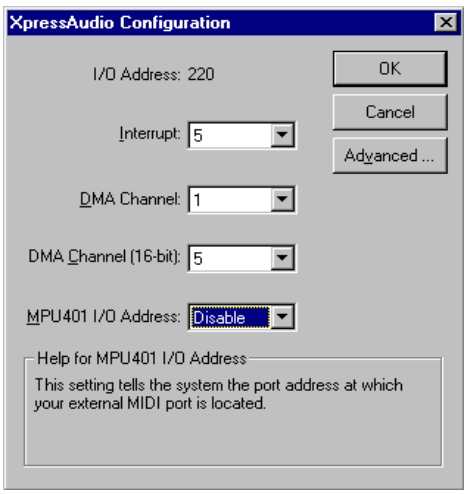


8. The Audio driver should now be listed as shown below. Click '*OK*' to accept.



9. I/O address, interrupt, and DMA channel may now be configured. An example is shown below.

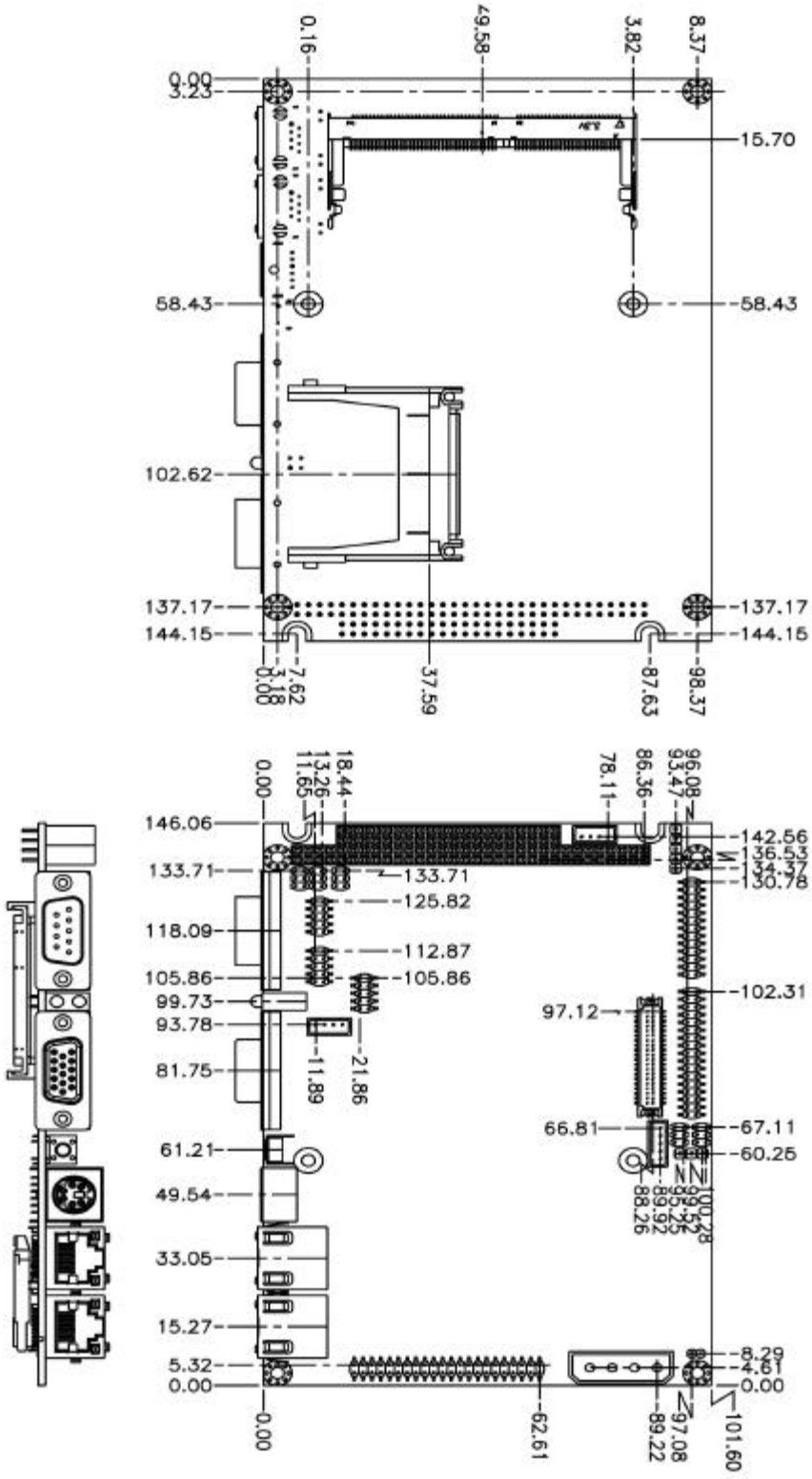




10. Click '*OK*' and close the '*Install Driver*' and '*Multimedia Properties*' windows by clicking the '*Close*' button in each window.

11. After closing the '*Multimedia Properties*' window, the computer must be restarted for the changes to take effect.

6. Measurement Drawing



Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: System Resources

Memory Map

The following table indicates memory map of EBC-3410. The address ranges specify the runtime code length.

Address Range	Description	Note
00000000h-0009FFFFh	System board extension for PnP BIOS	
000A0000h-000C7FFFh	XpressGRAPHICS	
00100000h-01BFFFFFh	System board extension for PnP BIOS	
40008000h-40010FFFh	System board extension for PnP BIOS	
40011000h-4001107Fh	XpressAUDIO PCI bridge	
40012000h-400120FFh	PCI bridge	
40018000h-407FFFFFh	System board extension for PnP BIOS	
40800000h-40FFFFFFh	XpressGRAPHICS	
41000000h-41017FFFh	System board extension for PnP BIOS	
DA000000h-DA03FFFFh	Intel ® GD82559ER PCI Adapter	
DA040000h-DA041FFFh	Intel ® GD82559ER PCI Adapter	
FFFC0000h-FFFFFFFFh	System board extension for PnP BIOS	

Note:

The usage of these I/O addresses depends on the choices made in the BCM setup screen. The I/O addresses are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

I/O – Map

The board incorporates a fully ISA Bus Compatible slave interface. The drive capabilities allow for up to four external PC/104 modules to be driven without external data buffers. The accessible I/O area on the ISA-bus is 64Kbytes with 16 address bits, whereas the accessible memory area is 16Mbytes with 24 address bits.

Certain I/O addresses are subject to change during boot as PnP managers may relocate devices or functions. The addresses shown in the table are typical locations.

I/O Port	Description	Note
0000h-000Fh	8237 compatible DMA controller 1	
0020h-0021h	8259 compatible programmable interrupt controller 1	
0040h-0043h	82C54 compatible Programmable timer 1	
0060h-0060h	8042 compatible keyboard-controller	
0061h-0061h	System buzzer	
0064h-0064h	8042 compatible keyboard-controller	
0070h-0071h	RTC clock and CMOS RAM	
0081h-0083h	DMA control	
0087h-0087h	DMA control	
0089h-008Bh	DMA control	
008Fh-0091h	DMA control	
00A0h-00A1h	Programmable interrupt controller 2	
00C0h-00DFh	DMA control	
00F0h-00FFh	Numeric processor	
01F0h-01F7h	Primary IDE controller (single FIFO)	
0200h-0200h	Gameport joystick	
0220h-022Fh	XpressAUDIO 16-bit sound	
0278h-027Fh	Parallel port 2	1
02F8h-02FFh	Serial port 2	1
0330h-0331h	XpressAUDIO 16-bit sound	
0378h-037Fh	Parallel port 1	1
0388h-038Bh	XpressAUDIO 16-bit sound	
03B0h-03BBh	XpressGRAPHICS	
03BCh-03BFh	Parallel port 3	1
03C0h-03DFh	XpressGRAPHICS	
03F2h-03F5h	Floppy disk controller	
03F6h-03F6h	Standard Dual PCI IDE Controller	
03F6h-03F6h	Primary IDE controller (single FIFO)	
03F8h-03FFh	Serial port 1	1
0480h-048Fh	PCI bus	
04D0h-04D1h	PCI bus	
0CF8h-0CFFh	PCI bus	
E000h-E03Fh	Intel ® GD82559ER PCI Adapter	
E400h-E43Fh	Intel ® GD82559ER PCI Adapter	

Note:

The usage of these I/O addresses depends on the choices made in the BCM setup screen. The I/O addresses are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

Interrupt Usage

The onboard CS5530A provides an ISA compatible interrupt controller with functionality as two 8259A interrupt controllers. The two controllers are cascaded to provide 13 external interrupts. Most of these are used by onboard devices, but a few are available through the PC/104 interface.

The actual interrupt settings depend on the PnP handler, the table below indicates the typical settings.

Interrupt	Description	Note
NMI	DRAM parity errors and IOCHCHK signal activation	
IRQ0	TIMER 0 interrupt	
IRQ1	Standard 101/102 keyboard	
IRQ2	Used for cascading IRQ8 - IRQ15	
IRQ3	Serial port 1 or 2 or IrDA communication Device	1
IRQ4	Serial port 1 or 2	1
IRQ5	XpressAUDIO 16-bit sound	1,2
IRQ6	Floppy disk controller	1
IRQ7	Parallel port	1
IRQ8	Real time clock	
IRQ9	Available for PC/104 interface	
IRQ10	IRQ holder for PCI steering	
IRQ10	Intel ® GD82559ER PCI Adapter	1,2
IRQ11	IRQ holder for PCI steering	
IRQ11	Intel ® GD82559ER PCI Adapter	1,2
IRQ12	Standard PS/2 port mouse	1
IRQ13	Numeric processor	
IRQ14	Standard dual PCI IDE controller	3
IRQ14	Primary IDE controller (single FIFO)	3
IRQ15	Available for PC/104 interface	

Note:

1. The usage of these interrupts depends on the choices made in the BCM setup screen. The interrupts are fully useable for PC/104 interface if the corresponding on-board unit is disabled in the BIOS setup.
2. These interrupt lines are managed by the PnP handler and are subject to change during system initialisation.
3. IRQ14 is routed directly from the IDE hard disk connector to the PC-AT bus.
4. Disabling the hard disk controller in the BCM setup screen may not release the interrupt line.

DMA-channel Usage

The DMA circuitry incorporates the functionality of two 8237 DMA controllers with seven programmable channels. The controllers are referenced DMA Controller 1 for channels 0-3 and DMA Controller 2 for channels 4-7. Channel 4 is by default used to cascade the two controllers.

Channels 0-3 are hardwired to 8-bit count-by-bytes transfers and channels 5-7 to 16-bit count-by-bytes transfers.

The onboard CS5530A provides 24-bit addressing with the 16 least significant bits [15:0] in the Current register and the most significant bits [24:16] in the Page register.

DMA-channel	Description	Note
DMA0	Available in PC/104 interface	
DMA1	XpressAUDIO 16-bit sound	
DMA2	Floppy disk controller	1
DMA3	Parallel port, if using ECP mode	1
DMA4	Used for cascading	
DMA5	XpressAUDIO 16-bit sound	
DMA6	Available for PC/104 interface	
DMA7	Available for PC/104 interface	

Note:

The usage of these DMA-channels depends on the choices made in the BCM setup screen. The DMA-channels are fully usable for PC/104 interface if the corresponding on-board unit is disabled in the setup screen.

Appendix C: Programming the Watchdog Timer

Introduction

The EBC-3410 onboard watchdog timer is based on an 8-bit counter. The time interval is from 16 seconds to 127 minutes with a resolution of 30 seconds. As soon as the timer is out, the system will generate a reset signal.

Configure Register

The EBC-3410 onboard watchdog timer function is integrated in the I/O chip, Winbond W83977F. If you would like to utilize this function in your program, you have to know how to program the 83977F configuration register. The W83977F I/O chip decode address is 3F0h. The index port and data port is 3F1h. The way to program the register is to write the register number to index port, then read / write data from / to data port.

The following procedures show how to program the W83977F register and use the watchdog function.

1. Unlock W83977F I/O chip and enter configuration mode.
2. Select Logical Device.
3. Select register number.
4. Read / Write data from / to register.
5. Lock W83977F I/O chip and exit from configuration mode.

Programming Watchdog Timer

To Unlock / Lock W83977F and Enter / Exit configuration mode is to write a specific value to I/O Port 3F0h as shown below.

Unlock W83977F: write value 87h to I/O port 3F0h twice.
Lock W83977F: write value aah to I/O port 3F0h.
Therefore, to unlock W83977F I/O chip and enter configuration mode, write twice unlock value (87h) to port 3F0h.

```
Ex: outportb(0x3f0, 0x87);
    outportb(0x3f0, 0x87);
```

Set register 30h of logical device 8 to 1 to activate the timer.
Logical Device 8: Register number 30h (CR30)
00h: timer inactive
01h: timer active

```
Write value 7 to port 3F0h          /* register 7 (logical device switch register)*/
Write value 8 to port 3F1h          /* write value 8 to enter logical device 8 */
Ex: outportb(0x3f0, 0x07);
    outportb(0x3f1, 0x08);
```

Write time-out value (01h ~ FFh) to timer register (F2h).
Logical Device 8: Register number F2h (CRF2)
00h: Time-out Disable
01h: Time-out occurs after 16 seconds
02h: Time-out occurs after 46 seconds
03h: Time-out occurs after 1 minute 16 seconds
04h: Time-out occurs after 1 minute 46 seconds
05h: Time-out occurs after 2 minutes 16 seconds

```
        .
        .
        .
```

FFh: Time-out occurs after 127 minutes 16 seconds

Write register number F2h to port 3F0h
Write time-out value to port 3F1h

```
Ex: outportb(0x3f0, 0xF2);          /* register F2 (Watchdog Timer) */
    outportb(0x3f1, 0x01);          /* time-out value 01 = 16 seconds */
```

Lock W83977F I/O chip, and exit configuration mode
Write lock value (AAh) to port 3F0h

```
 Ex: outportb(0x3f0, 0xAA);
```

The following shows two examples of programming the watchdog timer with 16 seconds time interval in both Micro-assembly and C language.

Demo Program 1 (Micro-Assembly Language)

```
;;=============================================================

;;  Title       : EBC-3410 Watchdog Timer Demo Program (16 seconds)

;; Company : BCM Advanced Research.

;; Date        : 10/04/2000

;;=============================================================


W83977_IO_PORT  EQU     3F0H
UNLOCK_ID          EQU     087h
LOCK_ID              EQU     0AAH

        .model  small
        .code
;;-----------------------------------------------------
;; Main Program start
;;-----------------------------------------------------
WatchDog PROC
;; Set Logic Device 8 active
        mov     bl, 8                   ;; Logic Device 8
        mov     al, 30h                 ;; Register 30h
        mov     ah, 01h                 ;; Active --> 01h, Inactive --> 00h
        call    W977_Register_Set


;; Set watchdog time-out value = 1  (16 seconds)
        mov     bl, 8                   ;; Logic Device 8
        mov     al, 0F2h                ;; Register F2h
        mov     ah, 01h                 ;; 01h ~ FFh  = 0:16 ~ 127:16
        call    W977_Register_Set

        mov     ah,4ch                  ;; Return to DOS
        int     21h
        ret
WatchDog ENDP
```

```
;;-------------------------------------------------


;;-------------------------------------------------
;; unlock W83977 register configuration mode
;;-------------------------------------------------
Unlock_977 proc
        cli
        push    ax
        push    dx
        mov     al, UNLOCK_ID
        mov     dx, cs:W83977_IO_PORT
        out     dx, al                  ;; write Unlock_ID to w83977 twice
        out     dx, al
        jmp     $+2
        jmp     $+2
        pop     dx
        pop     ax
        ret
Unlock_977 endp
;;-------------------------------------------------

;;-------------------------------------------------
;; lock w83977 register configuration mode
;;-------------------------------------------------
Lock_977 proc
        push    ax
        push    dx
        mov     dx, cs:W83977_IO_PORT
        mov     al, LOCK_ID
        out     dx, al
        pop     dx
        pop     ax
        ret
Lock_977 endp
;;-------------------------------------------------
```

```
;;-------------------------------------------------
;; Select W83977 I/O chip Logic Device
;; bl : Device Number
;;-------------------------------------------------
Set_Device proc
        push    ax
        push    dx
        mov     dx, cs:W83977_IO_PORT
        mov     al, 07h
        out     dx, al
        inc     dx
        mov     al, bl
        out     dx, al
        pop     dx
        pop     ax
        ret
Set_Device endp
;;-------------------------------------------------

;;-------------------------------------------------
;; Write data to W83977 Register
;;  al : register number
;;  ah : data
;;  bl : device number
;;-------------------------------------------------
W977_Register_Set PROC
        push    dx
        call    Unlock_977
        call    Set_Device
        mov     dx, cs: W83977_IO_PORT
        out     dx, al
        mov     al, ah
        inc     dx
        out     dx, al
        call    Lock_977
        pop     dx
        ret
W977_Register_Set ENDP
;;-------------------------------------------------
      end
```

Demo Program 2 (C Language)

```
//=============================================================

//  Title       : EBC-3410 Watchdog Timer Test Utility

// Company : BCM Advanced Research.

// Version    : 1.0

// Date        : 10/04/2000

// Compiler  : Borland C ++

//=============================================================


#include <stdio.h>
#include <stdlib.h>
#include <conio.h>

#define IO_INDEX_PORT      0x3F0
#define IO_DATA_PORT       0x3F1
#define UNLOCK_DATA       0x87
#define LOCK_DATA          0xAA
#define DEVICE_REGISTER 0x07

void EnterConfigMode()
{
   outportb(IO_INDEX_PORT, UNLOCK_DATA);
   outportb(IO_INDEX_PORT, UNLOCK_DATA);
}

void ExitConfigMode()
{
   outportb(IO_INDEX_PORT, LOCK_DATA);
}

void SelectDevice(unsigned char device)
{
   outportb(IO_INDEX_PORT, DEVICE_REGISTER);
   outportb(IO_DATA_PORT, device);
}

unsigned char ReadAData(short int reg)
{
   outportb(IO_INDEX_PORT, reg);
   return (inportb(IO_DATA_PORT));
}
```

```
void WriteAData(unsigned char reg, unsigned char data)
{
   outportb(IO_INDEX_PORT, reg);
   outportb(IO_DATA_PORT, data);
}

void SetWatchDogTime(unsigned char time_val)
{
   EnterConfigMode();
   SelectDevice(8);
      //Set Register F2
            //Set Watch-Dog Timer 1~ 256 steps
   WriteAData(0xF2, time_val);
   ExitConfigMode();
}

void main(int argc, char* argv[])
{
  int time_value=0;
  char *ptr;

  printf("WinBond 83977F/AF WatchDog Timer Test Utility Version 1.0 \n");
  printf("Copyright (C) 2000 BCM Advanced Research c.\n");
  printf("(Support EBC-3410 only and the system will be reset)\n");
  if (argc == 1)
   { printf("\n Syntax: 3412WD  [step] \n");
     printf(" step range : 1 ~ 256 steps \n");
     printf(" timer range: 0:16 ~ 127:16 (min:sec) \n");
     return ;
    }
  if (argc > 1)
   {
     ptr = argv[1];
     time_value = atoi(ptr);
   }
  if (time_value > 0 && time_value < 256)
   {
     SetWatchDogTime((unsigned char) time_value);
     printf("Watch Dog reset Timer set up : %02d:%02d ",(time_value-1)/2,
                                          ((time_value-1)%2)*30+16);
   }
}
```

Appendix D: AWARD BIOS Error Message

During the power-on self test (POST), the BIOS either sounds a beep code or displays a message when it detects a correctable error.

Following is a list of POST messages for the ISA BIOS kernel. Specific chipset ports and BIOS extensions may include additional messages. An error message may be followed by a prompt to press F1 to continue or press DEL to enter Setup.

Beep

Currently the only beep code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps.

BIOS ROM Checksum Error – System Halted

The checksum of the BIOS code in the BIOS chip is incorrect, indicating the BIOS code may have become corrupt. Contact your system dealer to replace the BIOS.

CMOS Battery Failed

CMOS battery is no longer functional. Contact your system dealer for a replacement battery.

CMOS Checksum Error – Defaults Loaded

Checksum of CMOS is incorrect, so the system loads the default equipment configuration. A checksum error may indicate that CMOS has become corrupt. This error may caused by a weak battery. Check the battery and replace if necessary.

CPU at nnnn

Displays the running speed of the CPU.

Display Switch Is Set Incorrectly.

The display switch on the motherboard can be set to either monochrome or color. This message indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Press ESC to Skip Memory Test

The user may press Esc to skip the full memory test.

Floppy Disk(s) Fail

Cannot find or initialize the floppy drive controller or the drive. Make sure the controller is installed correctly. If no floppy drives are installed, be sure the Diskette Drive selection in Setup is set to NONE or AUTO.

Hard Disk(s) Initializing; Please Wait a Moment...

Some hard drives require extra time to initialize.

Hard Disk(s) Install Failure

Cannot find or initialize the hard drive controller or the drive. Make sure the controller is installed correctly. If no hard drives are installed, be sure the Hard Drive selection in Setup is set to NONE.

Hard Disk(s) Diagnosis Fail

The system may run specific disk diagnostic routines. This message appears if one or more hard disks return an error when the diagnostics run.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are pressed during POST. To purposely configure the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. The BIOS then ignores the missing keyboard during POST.

Keyboard Is Locked Out – Unlock The Key

This message usually indicates that one or more keys have been pressed during the keyboard tests. Be sure no objects are resting on the keyboard.

Memory Test

This message displays during a full memory test, counting down the memory areas being tested.

Memory Test Fail

If POST detects an error during memory testing, additional information appears giving specifics about the type and location of the memory error.

Override Enabled – Defaults Loaded

If the system cannot boot using the current CMOS configuration, the BIOS can override the current configuration is a set of BIOS defaults designed for the most stable, minimal-performance system operations.

Press TAB to Show POST Screen

System OEMs may replace the Award BIOS POST display with their own proprietary display. Including this message in the OEM display permits the operator to switch between the OEM display and the default POST display.

Primary Master Hard Disk Fail

POST detects an error in the primary master IDE hard drive.

Primary Slave Hard Disk Fail

POST detects an error in the secondary master IDE hard drive.

Resuming from Disk, Press TAB to Show POST Screen

Award offers a save-to-disk feature for notebook computers. This message may appear when the operator re-starts the system after a save-to-disk shutdown. See the Press TAB ... message above for a description of this feature.

Secondary Master Hard Disk Fail

POST detects an error in the primary slave IDE hard drive.

Secondary Slave Hard Disk Fail

POST detects an error in the secondary slave IDE hard drive.

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Appendix E: AWARD BIOS POST Codes

Note: ISA POST codes are outputted to port address 80h

Code (Hex)	Name	Description
C0	Turn off Chipset Cache	OEM Specific-Cache control
1	Processor Test 1	Processor Status (1FLAGS) Verification. Tests the following processor status flags: carry, zero, sign, overflow. The BIOS sets each flag, verifies they are set, then turns each flagoff and verifies it is off.
2	Processor Test 2	Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00.
3	Initialize Chips	Disable NMI, PIE, AIE, UEI, SQWV. Disable video, parity checking, DMA. Reset math coprocessor. Clear all page registers, CMOS shutdown byte. Initialize timer 0, 1, and 2, including set EISA timer to a known state. Initialize DMA controllers 0 and 1. Initialize interrupt controllers 0 and 1. Initialize EISA extended registers.
4	Test Memory Refresh Toggle	RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
5	Blank video, Initialize keyboard	Keyboard controller initialization.
6	Reserved	
7	Test CMOS Interface and Battery Status	Verifies CMOS is working correctly, detects bad battery.
BE	Chipset Default Initialization	Program chipset registers with power on BIOS defaults.
C1	Memory presence test	OEM Specific-Test to size on-board memory
C5	Early Shadow	OEM Specific-Early Shadow enable for fast boot.
C6	Cache presence test	External cache size detection
8	Setup low memory	Early chip set initialization. Memory presence test. OEM chip set routines. Clear low 64K of memory. Test first 64K memory.
9	EARLY CACHE INITIALIZATION	Cyrix CPU initialization. Cache initialisation.
A	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL.

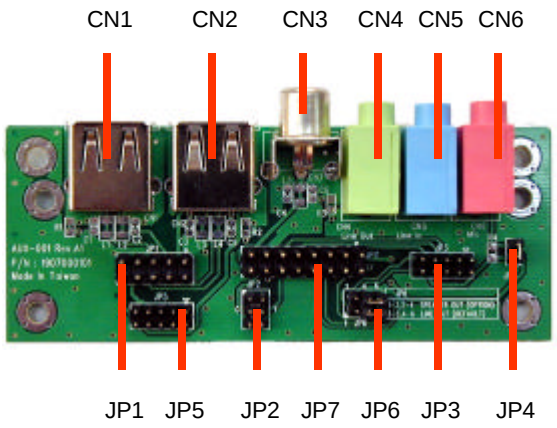
Code (Hex)	Name	Description
B	Test CMOS RAM Checksum	Test CMOS RAM Checksum, if bad, or insert key pressed. Load defaults.
C	INITIALIZE KEYBOARD	DETECT TYPE OF KEYBOARD CONTROLLER (OPTIONAL). Set NUM_LOCK status.
D	INITIALIZE VIDEO INTERFACE	Detect CPU clock. Read CMOS location 14h to find out type of video in use. Detect and initialize Video adapter.
E	Test Video memory	Test video memory, write sign-on message to screen. Setup shadow RAM – Enable shadow according to Setup.
F	Test DMA Controller 0	BIOS Checksum test. Keyboard detect and initialization.
10	Test DMA Controller 1	
11	Test DMA Page Registers	TEST DMA PAGE REGISTERS.
12-13	Reserved	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
15	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
16	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
17	Test Stuck 8259's Interrupt Bits	Turn off interrupts then verify no Interrupt mask register is on.
18	Test 8259 Interrupt Functionality	Force an interrupt and verify the interrupt occurred.
19	Test Stuck NMI Bits (Parity / IO Check)	Verify NMI can be cleared.
1A	DISPLAY CPU CLOCK	
1B-1E	RESERVED	
1F	SET EISA MODE	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests a clear EISA mode flag. Test EISA Configuration Memory Integrity (checksum & communication interface).
20	Enable Slot 0	Initialize slot 0 (System Board).
21-2F	Enable Slots 1-15	Initialize slot 1 through 15.
30	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.

Code (Hex)	Name	Description
31	Test Base and Extended Memory	Test base memory from 256K to 640K Extended Memory and extended memory above 1MB using various patterns. NOTE: This test is skipped in EISA mode and can be skipped with ESC key in ISA mode.
32	Test EISA Extended Memory	If EISA Mode flag is set then test EISA memory found in slots initialization. NOTE: This test is skipped in ISA mode and can be skipped with ESC key in EISA mode.
33-3B	Reserved	
3C	Setup Enabled	
3D	Initialize & Install Mouse	Detect if mouse is present, initialize mouse and install interrupt vectors.
3E	Setup Cache Controller	Initialize cache controller.
3F	Reserved	
BF	Chipset Initialization	PROGRAM CHIPSET REGISTERS WITH SETUP VALUES.
40		Display virus protect disable or enable.
41	Initialize Floppy Drive & Controller	Initialize floppy disk drive controller and any drives.
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drives.
43	Detect & Initialize Serial / Parallel Ports	Initialize any serial and parallel ports (also game port).
44	Reserved	
45	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
46	Reserved	
47	Reserved	
48-4D	Reserved	
4E	Manufacturing POST Loop or Display Messages	Reboot if Manufacturing POST Loop pin is set. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST) and enter Setup.
4F	Security Check	Ask password security (optional).
50	Write CMOS	Write all CMOS values back to RAM and clear screen.
51	Pre-boot Enable	Enable parity checker. Enable NMI, Enable cache before boot.
52	INITIALIZE OPTION ROMS	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
53	Initialize Time Value	INITIALIZE TIME VALUE IN 40H: BIOS AREA.

Code (Hex)	Name	Description
60	Setup Virus Setup	Setup Virus protect according to Setup.
61	SET BOOT SPEED	Set system speed for boot.
62	SETUP NUMLOCK	Setup Numlock status according to Setup.
63	BOOT ATTEMPT	Set low stack. Boot via INT 19h.
B0	SPURIOUS	If interrupt occurs in protected mode.
B1	UNCLAIMED NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot.
E1-EF	SETUP PAGES	E1 – Page 1, E2 – Page 2, etc.
FF	BOOT	

Appendix F: Audio / USB Daughter Board User's Guide

Jumper & Connector Layout



Jumper & Connector List

Jumpers		
Label	**Function**	**Note**
JP1	2.54mm pitch USB connector for Mini module series	5 x 2 header, pitch 2.54mm
JP2	Reserve for S-terminal testing	3 x 2 header, pitch 2.0mm
JP3	Audio connector for Micro module series	5 x 2 header, pitch 2.0mm
JP4	Reserved	
JP5	2.00mm pitch USB connector for Micro module series	5 x 2 header, pitch 2.0mm
JP6	Line out / Speaker out select	1-3, 2-4 Speaker out 3-5, 4-6 Line out (Default)
JP7	TV / Audio connector for Mini module series	8 x 2 header, pitch 2.54mm

Connectors		
Label	**Function**	**Note**
CN1	USB 1 connector	
CN2	USB 2 connector	
CN3	TV output RCA jack	
CN4	Line out or Speaker out	Select by JP6
CN5	Line in	
CN6	Mic in	

Measurement Drawing